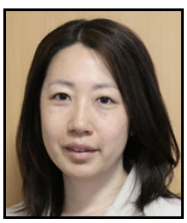
Session 6 Overview: *Image Sensors*

IMMD SUBCOMMITTEE

Session Chair: *Jun Deguchi, Toshiba, Kawasaki, Japan*

Session Co-Chair: *David Stoppa, Fondazione Bruno Kessler, Trento, Italy*

The session presents advances in image sensors, covering emerging topics like 3D stacking, organic photoconductive film technologies and single-photon detectors as well as new trends in high-resolution cameras. The first two papers integrate organic photoconductive film with a CMOS image sensor to enable wide intrascene dynamic range, global shutter, multiple exposure and variable sensitivity image capture. The next two papers present high-resolution CMOS image sensors for airborne mapping applications and DSLR cameras. Single-photon avalanche photodiodes for long-range time-of-flight and low-light imaging applications are presented in the fifth and sixth papers. Finally, the last three papers report on 3D-stacked CMOS image sensors for mobile and emerging high-end applications.



1:30 PM

6.1 An Over 120dB Simultaneous-Capture Wide-Dynamic-Range 1.6e^- Ultra-Low-Reset-Noise Organic-Photoconductive-Film CMOS Image Sensor

K. Nishimura, Panasonic, Moriguchi, Japan

In Paper 6.1, Panasonic presents an image sensor based on organic photoconductive film. The sensor features over 120dB intrascene dynamic range, a full well capacity of 600ke^- on 3.3.V pixel power supply and a random noise of 5.4e^-.

2:00 PM

6.2 210ke^- Saturation Signal 3µm-Pixel Variable-Sensitivity Global- Shutter Organic Photoconductive Image Sensor for Motion Capture

S. Shishido, Panasonic, Moriguchi, Japan

In Paper 6.2, Panasonic proposes a global shutter imager based on organic photoconductive film exploiting in-pixel gain switching featuring 210ke^- saturation in a 3µm-pitch pixel.

2:15 PM

6.3 105×65mm^2 391Mpixel CMOS Image Sensor with >78dB Dynamic Range for Airborne Mapping Applications

J. Bogaerts, CMOSIS NV, Antwerp, Belgium

In Paper 6.3, CMOSIS NV presents a 105×65mm^2 391Mpixel CMOS image sensor for airborne mapping applications. The sensor based on 3.9µm-pitch pixels exhibits a 3.7e^- rms noise and 78dB dynamic range.

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2:30 PM

6.4 An APS-H-Size 250Mpixel CMOS Image Sensor Using Column Single-Slope ADCs with Dual-Gain Amplifiers

H. Totsuka, Canon, Kawasaki, Japan

In Paper 6.4, Canon presents an APS-H size 250Mpixel CMOS image sensor. The sensor is fabricated with a 0.13µm CMOS technology and is based on 1.5µm-pitch pixels and single-slope column ADCs with dual-gain amplifiers featuring 6dB wider dynamic range and 75% shorter conversion time than a conventional single-slope ADC.

3:15 PM

6.5 A 64×64-Pixel Digital Silicon Photomultiplier Direct ToF Sensor with 100MPhotons/s/pixel Background Rejection and Imaging/Altimeter Mode with 0.14% Precision up to 6km for Spacecraft Navigation and Landing

M. Perenzoni, Fondazione Bruno Kessler, Trento, Italy

In Paper 6.5, Fondazione Bruno Kessler presents a 64×64-pixel Time-of-Flight 3D imager for spacecraft navigation and landing. The sensor achieves a precision of 0.14% up to 6km distance and a background rejection up to 100Mphotons/s/pixel.

3:45 PM

6.6 A 1280×720 Single-Photon-Detecting Image Sensor with 100dB Dynamic Range Using a Sensitivity-Boosting Technique

M. Usuda, Panasonic, Nagaokakyo, Japan

In Paper 6.6, Panasonic proposes a 1280×720-pixel array achieving single-photon detection capability thanks to a modified BSI pinned-photodiode device that can operate as in conventional photodiode and avalanche photodiode modes.

4:00 PM

6.7 A 1.2e$^-$ Temporal Noise 3D-Stacked CMOS Image Sensor with Comparator-Based Multiple-Sampling PGA

K. Shiraishi, Toshiba, Kawasaki, Japan

In Paper 6.7, Toshiba describes a 3D-stacked image sensor for mobile applications exploiting low-noise PGA and low-power single-slope ADC to achieve a temporal noise of 1.2e$^-$ at 20fps and 32× multiple sampling.

4:15 PM

6.8 A 1.5V 33Mpixel 3D-Stacked CMOS Image Sensor with Negative Substrate Bias

C. C-M. Liu, TSMC, Hsinchu, Taiwan

In Paper 6.8, TSMC describes a 33Mpixel 3D-stacked CMOS image sensor demonstrating 82.5% array-area to chip-area ratio and featuring 82.35µV$_{rms}$ noise at unitary gain.

4:45 PM

6.9 A 1.1µm 33Mpixel 240fps 3D-Stacked CMOS Image Sensor with 3-Stage Cyclic-Based Analog-to-Digital Converters

T. Arai, NHK Science & Technology Research Laboratories, Tokyo, Japan

In Paper 6.9, NHK Science & Technology Research Laboratories present a 33Mpixel 3D-stacked CMOS image sensor based on 12b 3-stage pipelined ADCs featuring 3.6e$^-$ temporal noise at 7.96Gpixel/s.

6.1 An Over 120dB Simultaneous-Capture Wide-Dynamic-Range 1.6e⁻ Ultra-Low-Reset-Noise Organic-Photoconductive-Film CMOS Image Sensor

Kazuko Nishimura, Yoshihiro Sato, Junji Hirase, Ryota Sakaida, Masaaki Yanagida, Tokuhiko Tamaki, Masayuki Takase, Hidenari Kanehara, Masashi Murakami, Yasunori Inoue

Panasonic, Moriguchi, Japan

Image sensors are increasingly becoming key devices for various applications (in-vehicle, surveillance, medical, and so on). To realize the best possible imaging and sensing performance, there is growing demand for extended dynamic range that can precisely reproduce color tone. Several conventional papers have described methods for enhancing dynamic range, such as multiple exposures in a frame [1] and a lateral overflow integration capacitor [2,3]. However, all these techniques realize a 100-to-200dB dynamic range by synthesizing multiple exposures, with asynchronism between multiple exposures causing time distortion. Thus, a simultaneous-capture wide dynamic range (SCWDR) over 100dB is desired.

To solve this problem, we develop a CMOS image sensor that has a 123.8dB SCWDR, a 600ke⁻ full-well capacity, and a 1.6e⁻ ultra-low reset noise, with an organic-photoconductive-film (OPF) laminated on pixel circuits, using a 65nm CMOS process. The pixel structure of the OPF image sensor is different from that of a common silicon image sensor. In a silicon sensor, both photoelectric conversion and charge storage are executed by the photodiode (PD). This means that sensitivity and full-well capacity are limited by the size and quantum efficiency of the PD. On the other hand, in an OPF image sensor, photoelectric conversion is done by the OPF, and charge is stored in the Floating Diffusion (FD) node capacitance. These two parts are completely independent. Moreover, the light absorption performance of the OPF is more than 10× higher than that of a silicon PD [4]. Therefore, an OPF image sensor realizes both high sensitivity and high saturation. In this work, we report a pixel structure, called "Dual-Sensitivity Pixel (DS-Pixel)," using an OPF image sensor structure in which sensitivity and saturation can be set independently. In one DS-Pixel, two photoelectric-conversion parts, two charge-storage parts and two types of noise cancellers are designed for two cells: (1) a "High-Sensitivity Cell" in which high sensitivity for dark regions is important, but large full-well capacity is not necessary, and (2) a "High-Saturation Cell" in which large full-well capacity for bright regions is important, but reset noise is buried in shot noise. We designed different circuits for each cell. Consequently, our OPF image sensor with the DS-Pixel combines high performances of the two cells at the same time, so the SCWDR is significantly improved. Also, both cells are exposed simultaneously and the time distortion is eliminated. In dark regions, furthermore, the OPF image sensor has a specific problem. As the OPF image sensor stores charge at capacitance other than the PD, Correlated Double Sampling (CDS) cannot be used and reset noise is left on the FD node. Several techniques have been proposed to suppress reset noise, but the effect is limited [5]. We therefore also report a "Capacitive-Coupled Noise Canceller (CCNC)" that suppresses reset noise with high speed and high precision, to improve S/N characteristics of dark regions.

Figure 6.1.1 shows a block diagram of the OPF image sensor. Each pixel is a DS-Pixel. Every column is equipped with feedback amplifiers (FBAMP) for noise cancellation and A/D converters. At A/D converters, in order to keep S/N characteristics at all illuminance levels, several analog gains are set. The converted digital signals at 60fps are read out using a Sub-LVDS interface.

Figure 6.1.2 shows a cross-sectional image of the DS-Pixel and its schematic diagrams. Each pixel consists of "Cell1" and "Cell2". Cell1 is the High-Sensitivity Cell for dark subjects, and it consists of four transistors and two capacitors as a noise canceller (CCNC), with a high-sensitivity pixel electrode (PE1). Cell2 is the High-Saturation Cell for ultra-bright subjects, and it consists of three transistors and a large charge-storage capacitor, with a low-sensitivity pixel electrode (PE2). The charge-storage capacitance ratio between the two cells is designed to be 10:1 and the sensitivity ratio between the two cells is designed to be 1/10:1. The exposure periods are set to be simultaneous, therefore, a 100× wider SCWDR is achieved by the DS-Pixel compared to that of common silicon sensors. Figure 6.1.2 (upper right) shows the layout of the pixel electrodes. PE1 has a large area for high sensitivity, and PE2 has a small area to realize one-tenth the sensitivity of PE1. In addition, a shield electrode is inserted between the two cells to restrain the color mixture.

Moreover, we have developed a new high-k MIM (Metal-Insulator-Metal) capacitor with capacitance of 18fF/μm² and leakage current of 7.5×10^{-10}A/cm². In the OPF image sensor, high-performance devices can be vertically layered between the OPF and CMOS circuits. This allows the MIM to be layered as a capacitor C_{s1} for noise cancellation in Cell1 and as a charge-storage capacitor C_{s2} in Cell2. Consequently, we can reduce the pixel size by over 75% compared to that with DMOS capacitors. If a silicon sensor of similar pixel size could be designed, it would be necessary to reduce the PD area and to sacrifice sensitivity and saturation charge. Therefore, this OPF image sensor is able to achieve both a small pixel size and a wide SCWDR.

This structure is also an effective solution to resolve the problem of LED flicker for in-vehicle cameras. In this structure, the High-Saturation Cell can be exposed using a low-sensitivity exposure during the whole time, except the readout period. Therefore, every line of pixels can fully capture an LED light, and so the LED flicker image problem is prevented.

Figure 6.1.3 shows a schematic of the CCNC, which consists of four transistors and two capacitors (SF: amplifier Tr, SEL: select Tr, RST: reset Tr, FB: feedback Tr, C_s: stabilized capacitor, C_c: coupled capacitor) for the High-Sensitivity Cell. First, RST and FB are turned on at the same time and the FD node is set to the reset voltage; RST and FB are then turned off sequentially. During this time, reset noise from RST and FB is suppressed by use of a negative feedback loop that includes FB, which is bandwidth-controlled using V_{fb}. When the gain of the negative feedback loop is set to –A, reset noise of RST and FB can be suppressed proportionally to $1/(A\times C_c/C_{fd})$ and $1/\sqrt{(A\times C_s/C_c)}$, respectively. As a result, by setting A and C_s/C_c to maximum value, reset noise can be decreased, within 5μs, from 25e⁻ to 1.6e⁻, which is 12% of that by the conventional technique [5]. Moreover, the robustness and speed of noise cancellation are improved, by controlling FB, which is separated from the FD node using C_c.

A die micrograph is shown in Fig. 6.1.7. The OPF image sensor with a SCWDR of over 120dB is fabricated in a 65nm 1PS 3Cu 1Al CMOS technology. The OPF image sensor is designed with a pixel size of 6μm, a pixel number of $970^{H}\times550^{V}$, and realizes 60fps digital readout by the Sub-LVDS interface. Moreover, 3μm pixel size, $1940^{H}\times1100^{V}$ (Full HD) resolution, and 60fps frame rate can be realized by replacing the DMOS capacitor with a high-k MIM capacitor. (Pixel size can be reduced by 75% and thus resolution can be quadrupled.)

Figure 6.1.4 shows the photoelectric conversion characteristics. Full-well capacity is 600ke⁻ on a 3.3V pixel power supply. The sensor's random noise is 5.4e⁻. The sensitivity ratio between the two cells is 14:1. A SCWDR of 123.8dB is achieved. Moreover, the use of typical multiple exposures provides a potential dynamic range of 180dB.

Figure 6.1.5 shows the sample images captured by the OPF image sensor with the DS-Pixel. The precise tone in the whole ranges is reproduced by weighting, using data from the two cells.

Finally, Fig. 6.1.6 lists the performance summary of the OPF CMOS image sensor, along with other state-of-the-art image sensors. Its SCWDR of 123.8dB, full-well capacity of 600ke⁻ and reset noise of 1.6e⁻ are the highest performances in the figure and will contribute to applications that require high-speed sensing.

Acknowledgment:
We would like to thank FUJIFILM Corporation for providing organic semiconducting materials and engineers in Panasonic Semiconductor Solution Co. for supporting chip design. And we would like to express special thanks to Yoshiyuki Matsunaga for encouragement and discussion throughout this work.

References:

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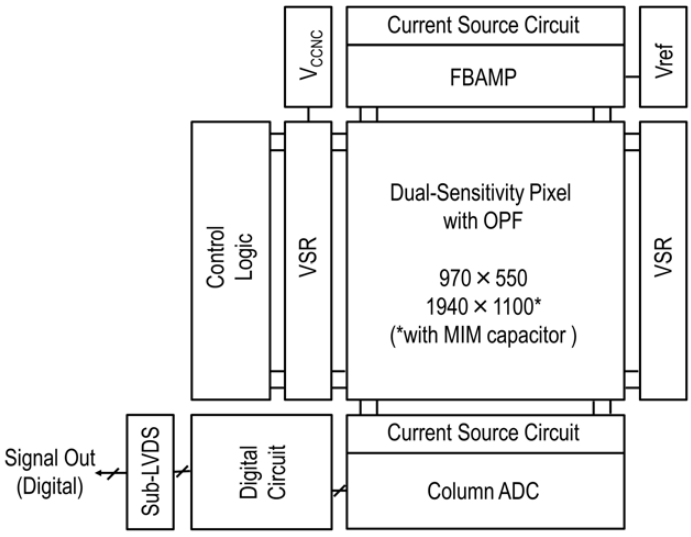

Figure 6.1.1: Block diagram of the OPF image sensor.

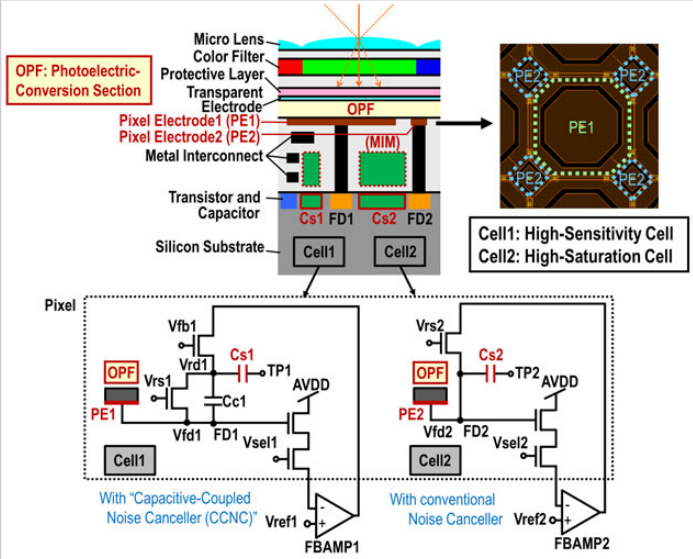

Figure 6.1.2: Cross-section and schematic of DS-Pixel.

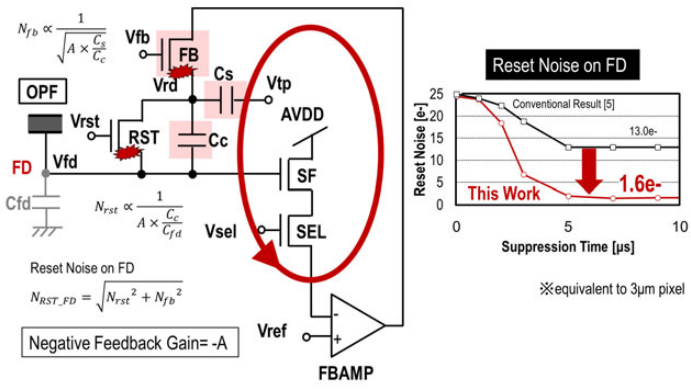

Figure 6.1.3: Schematic of CCNC.

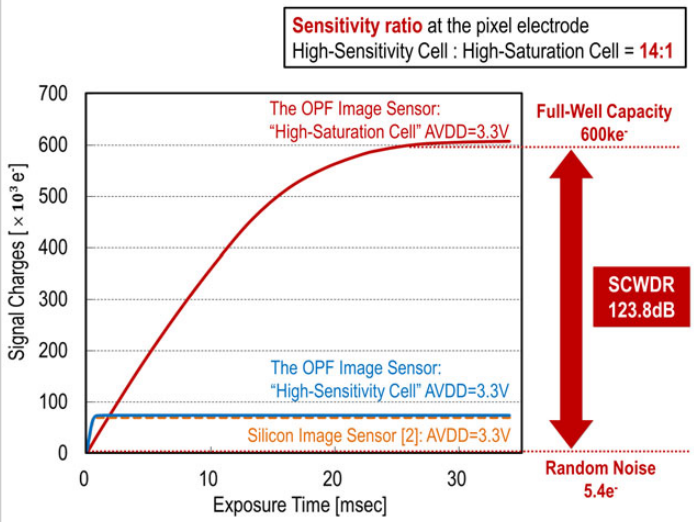

Figure 6.1.4: Photoelectric conversion characteristics.

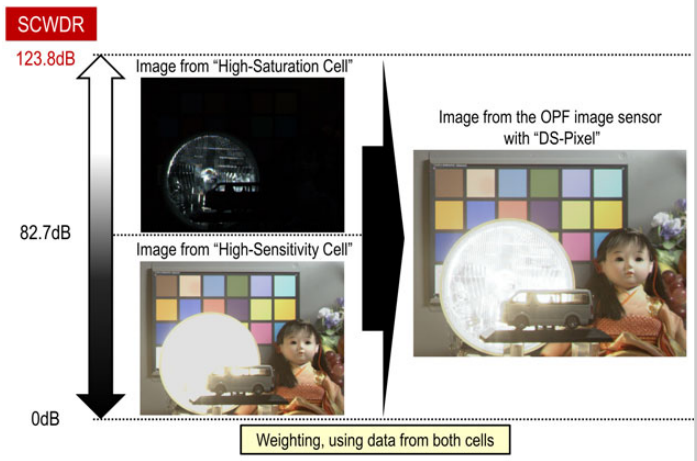

Figure 6.1.5: Typical images captured by DS-Pixel.

	This work	[1]	[2]	[3]
Chip Size [mm × mm]	14.97 × 10.27	---	5.4 × 1.8	2.6 × 2.6
Pixel Size [µm × µm]	6 × 6 3 × 3*	7.6 × 7.6	5.5 × 5.5	20 × 20
Number of Pixels	970 × 550 1940 × 1100*	96 × 96	360 × 1680	64 × 64
Frame Rate [fps]	60	15	---	---
Process Technology	65nm 1PS3Cu1Al CMOS	0.18um CMOS	0.18um 1PS5Metal CMOS	0.35um 2PS3Metal CMOS
SCWDR [dB]	123.8	87	104	100
WDR [dB] (by using exposure timing)	180	140	---	169 207 (with readout tech)
Full-Well Capacity [e-]	600k	---	76k	---
Random Noise [e-]	5.4	---	0.46	---
Reset Noise [e-]	1.6	---	---	---

*with MIM capacitor

Figure 6.1.6: Performance summary.

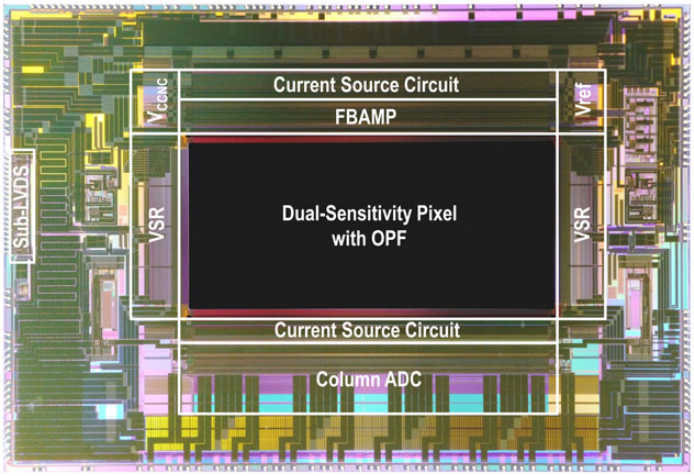

Figure 6.1.7: Chip micrograph.

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6.2 210ke⁻ Saturation Signal 3μm-Pixel Variable-Sensitivity Global-Shutter Organic Photoconductive Image Sensor for Motion Capture

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Panasonic, Moriguchi, Japan

Image sensors for applications such as machine vision, in-vehicle cameras, and surveillance cameras require a global shutter (GS) function. GS functions are an increasingly powerful technology driver, not only for solving imaging problems caused by rolling shutter distortion or flash bands, but also for use in sensing applications [1]. Conventional CMOS image sensors (CIS) with GS functions require storage located near the photoelectric conversion area [2-3], and the two-stage transferring pixel structures required to suppress kT/C noise need two storage nodes and extra transistors. This makes it difficult, in GS pixels, to simultaneously shrink the pixel size and enlarge the saturation signal.

On the other hand, the light absorption coefficient of organic photoconductive film (OPF) image sensors is over 10× larger than that of Si photodiodes, and signal charge is accumulated in the floating diffusion (FD) node that can be separated from the OPF [5-6]. FD and OPF can be vertically stacked, so this structure allows additional circuits in each pixel. Figure 6.2.1 shows a comparison of the saturation signal of an OPF image sensor with that of a conventional CMOS image sensor. The unique features of OPF image sensors make high saturation compatible with small pixel size.

We report high-saturation OPF image sensors with GS function by modulation of a voltage applied to the OPF. By implementation of photoelectric conversion controlled (PCC) GS and an in-pixel gain switching circuit, we develop an OPF image sensor with a 210ke⁻ saturation signal in a 3μm pixel.

A cross-sectional image and a schematic of PCC GS pixel are shown in Fig. 6.2.2. The photoelectric conversion efficiency of the OPF is controlled by modulating a voltage applied to a tin-doped indium oxide (ITO) electrode, realizing PCC GS operation and global sensitivity control. If the voltage applied to the ITO electrode is higher, then the shutter is open: optically generated electrons and holes are separated by an electric field, and holes are collected by a pixel electrode. If the voltage applied to the ITO electrode is lower, then the shutter is closed: optically generated electrons and holes recombine and are immediately extinguished. A signal carrier is kept stored in FD during PCC GS operation, so there is no need to add storage circuit and capacitors to the pixel. The vertical device structure in which photoelectric conversion area and storage node are not placed in the same plane and have a sufficiently high recombination speed are advantageous to lower parasitic light sensitivity (PLS).

Furthermore, a key feature of an OPF image sensor is that it allows additional pixel circuits, for example of capacitance C_s in the pixel for noise-cancelling operation and saturation extension, as shown in Fig. 6.2.2. By adding a capacitor C_s to the FD node while turning on the reset transistor RST, FD conversion gain is reduced to $1/(C_{fd}+C_s)$, which increases the saturation signal. Moreover, the additional transistors (SF2 and SEL2) increase the saturation signal when SF2 is used as a capacitor and improves speed and 1/f noise due to g_m increase and transistor size expansion when SF2 is used as an amplifier. When SEL2 is off, SF2 is used as a capacitor. A larger capacitance is obtained by setting the drain voltage of SF2 to AVSS rather than to AVDD. To avoid increasing parasitic capacitance of the vertical signal line, the source node of SEL2 should be connected to the drain node of SEL. When SEL2 is on, SF2 is also used as an amplifier and g_m becomes a factor of $\sqrt{(1+W_{sf2}/W_{sf})}$, i.e., 10× larger, where W_{sf} and W_{sf2} are the gate widths of SF and SF2, respectively.

Figure 6.2.3 shows a schematic of the pixel readout operation using a dual vertical signal line VSIG. Every odd-numbered row and even-numbered row has a common VSIG and a feedback line, FB_OUT. VSIG is used for column feedback during the electronic shutter and pixel reset operation, and VSIG is used as output line during the signal level or reset level readout. The sensor speed is therefore limited by these two reset times for electronic shutter and pixel reset or number of VSIG and FB_OUT.

For high-speed operation, we propose a pixel-separated reference readout process that does not use VSIG during reference level acquisition for correlated double sampling (CDS). Reference voltage VREF is connected to a comparator for single-slope ADC through sw_VREF. In a conventional CIS, VSIG must be used for signal level and reset level readout to subtract threshold voltage variation of in-pixel source-follower transistors. However, in an OPF, the image sensor pixel reset voltage is fixed to VREF. Readout through VSIG is therefore not necessary, and this makes it possible to separate the comparator from the pixel area by sw_VSIG. The number of reset operations is reduced from two to one, and high-speed operation is enabled. Compared to normal readout timing, the H cycle can be shortened from 13 to 7μs in the same way as an electronic shutter, and the frame rate can be improved from 60 to 100fps, since feedback reset FB RST before reference read is skipped.

Moreover, readout from an OFP image sensor is nondestructive, since there is no need for a transfer action from the OPF and accumulated charge is stored directly in the FD node. Nondestructive readout enables, for example, image monitoring during bulb photography to prevent under- or over-exposure in digital single-lens reflex (DSLR) cameras. A nondestructive read with no electrical shutter can shorten the H cycle to 4μs, and sensor speed is limited by interface circuitry or ADC speed, not by the H cycle.

Figure 6.2.4 shows the multiple-exposure sensor operated with: (a) fixed sensitivity and (b) variable sensitivity. PCC GS operation is executed by applying a pulse voltage to ITO, and applying multiple pulses enables multiple exposures. ITO voltage control starts during the V blanking period. The sensor frame rate is determined by the inverse of the sum of exposure time and readout scanning time. Changing the pulsed voltage in each exposure enables variable-sensitivity multiple exposure. Multiple exposure with fixed sensitivity cannot detect the direction of motion, but variable-sensitivity multiple exposure can, from a change in object brightness. To lower parasitic light sensitivity, the ITO voltage should be equal to the pixel reset voltage.

A chip micrograph is shown in Fig. 6.2.7. The OPF image sensor is fabricated in a 65nm 1P 3Cu 1Al CMOS process. The chip size is 15×10mm^2 and the pixel is 3×3μm^2 and the effective pixels are 1,920×1,080. A single-slope ADC is implemented in each column, and the converted digital value stored in digital memory is read out by sub-LVDS buffer after parallel-to-serial conversion. The ITO voltage controller placed outside of the chip is synchronized with the sensor readout by an on-board FPGA.

Figure 6.2.5 compares chip characteristics. We realize a saturation signal of 51.1ke⁻ at 3.3V pixel voltage in normal mode, and 210ke⁻ by using C_s. The saturation signal per unit square is 9.6× or more than that in other studies. PLS is -106dB even though there is no additional light shield structure.

Figure 6.2.6 shows images captured by PCC GS operation and variable-sensitivity multiple exposure. There is no distortion in PCC GS mode, unlike the severe distortion in rolling-shutter mode. Charge recombination time of PCC GS is shorter than 1μs, making it fast enough for image capture. It provides image capture at a high interval speed of 10μs, which is equivalent to over 100,000fps in multiple-exposure mode. We can also get several images of different exposure times in one picture by changing pulse duty, and character can be well recognized by choosing optimum exposure time as shown in Fig. 6.2.6. In variable-sensitivity multiple-exposure mode, the voltage applied to ITO increases with time, and direction of motion can be detected by an acquired object's signal level. This high-saturation PCC GS sensor enables detection of object movement, even if the background is quite bright. This emerging technique for acquiring variable-sensitivity multiple exposures using PCC GS opens to the way to motion capture and new sensing applications.

Acknowledgments:
The authors would like to thank FUJIFILM Corporation for supplying organic photoconductive materials and technical supports.

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[6] M. Ishii, et al., "An Ultra-low Noise Photoconductive Film Image Sensor With a High-speed Column Feedback," *Dig. Symp. VLSI Circuits*, pp. C8–C9, June 2013.

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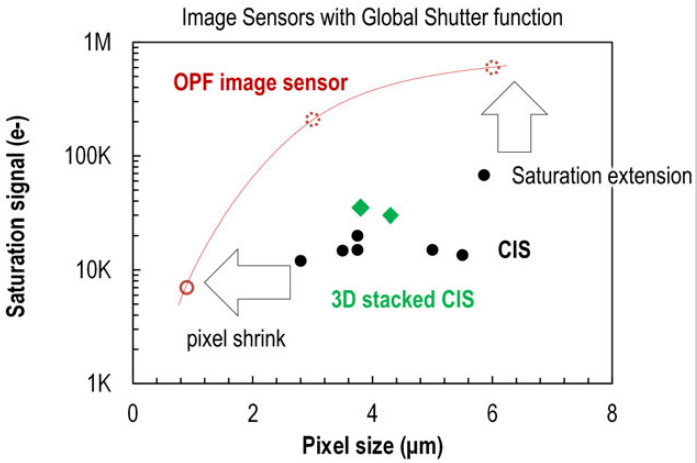

Figure 6.2.1: Saturation signal in GS sensors.

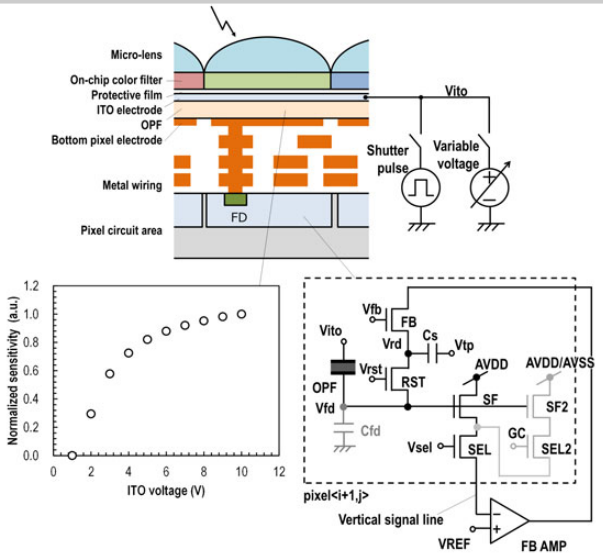

Figure 6.2.2: Cross-sectional image and schematic.

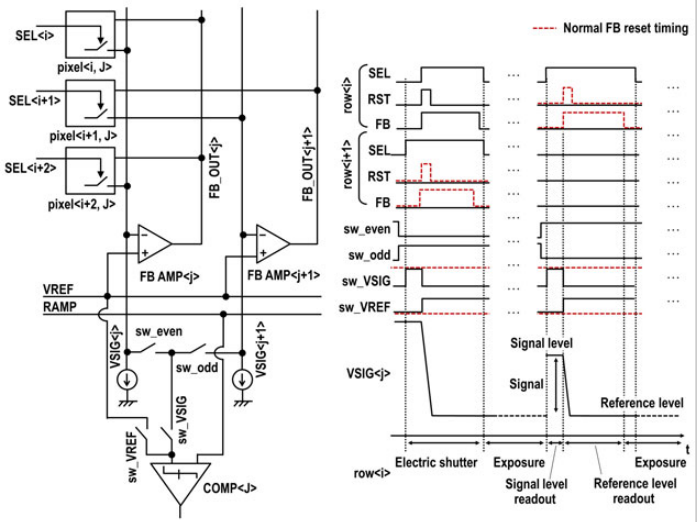

Figure 6.2.3: Schematic of pixel operation.

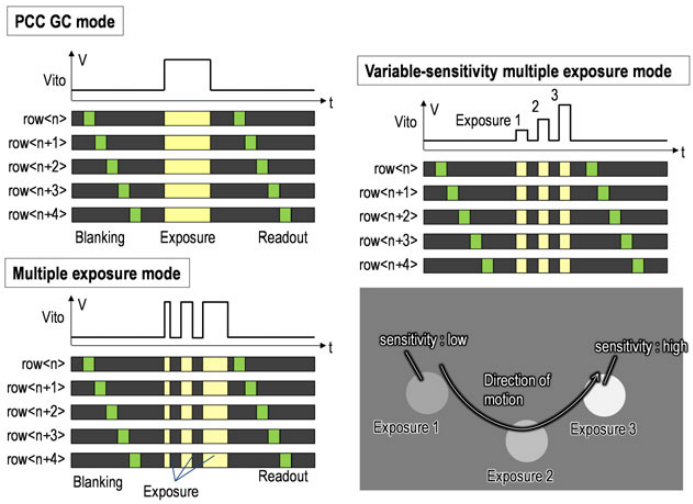

Figure 6.2.4: Sensor operation.

	This work	[4]	[3]	[2]
Device Configuration	OPF+CMOS	3D stacked CMOS	CMOS	CMOS
Process	65nm CMOS 1P3Cu1Al	0.18μm 1P6M /0.13μm 1P6M	110 nm 2Cu /90nm 3Cu1Al	90nm 1P5M +Light shield
Pixel count	1,920 x 1,080 (effective)	4,608 x 3,480 (effective)	-	10M (single) 5M (dual)
Pixel size [μm x μm]	3.0 x 3.0	3.8 x 3.8	3.5 x 3.5	5.86 x 5.86
Saturation signal [e-]	51.1k (normal) 77.5k (w/SF2) 210.2k (w/Cs)	35k	14.8k	32.2k (single) 67.7k (dual)
Dynamic range [dB]	81.3	-	58.5	76.5 (single) 83.0 (dual)
Random noise [e-]	4.4	-	17.6	4.8
Frame rate [fps]	60@2M	5@16M	350@12M	33.3@5M
Parasitic light sensitivity [dB]	-106dB	-180dB	-74dB	-100dB
Saturation signal /pixel area [e-/μm²]	5,678 (normal) 8,615 (w/SF2) 23,333 (w/Cs)	2,423	1,208	938 (single) 1,972 (dual)

Figure 6.2.5: Comparative table and chip characteristics.

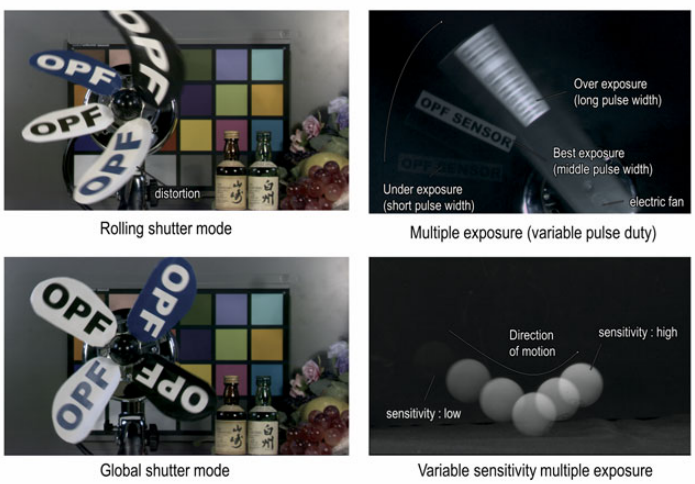

Figure 6.2.6: Captured image by fabricated OPF sensor.

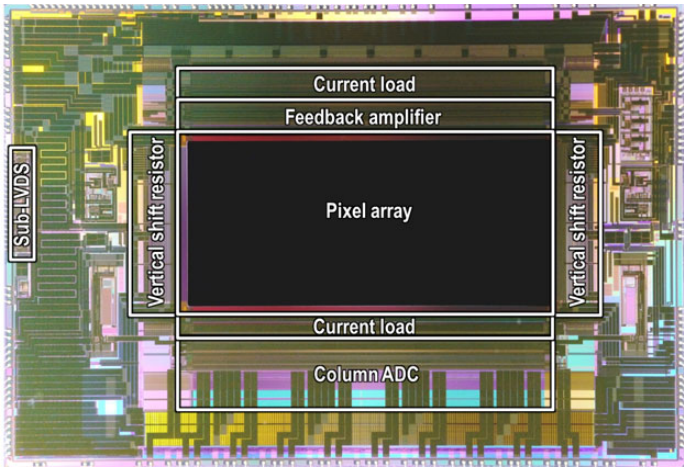

Figure 6.2.7: Chip micrograph.

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6.3 105×65mm² 391Mpixel CMOS Image Sensor with >78dB Dynamic Range for Airborne Mapping Applications

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In today's airborne mapping applications, there is a strong push towards higher-resolution sensors for high-end digital systems. This large-format sensor development aims to reduce the data acquisition (flight) time and cost, leading to higher productivity for the end-user. Due to the increased sensor resolution, these new systems allow higher flight altitude for the same ground sampling distance (GSD), thereby covering substantially larger swath width (distance covered across track during flight). Alternatively, at similar altitude, the system will deliver higher ground resolution. The described sensor exceeds the highest pixel count of sensors used for aerial mapping applications reported in a recent survey paper [1].

Figure 6.3.1 shows the sensor architecture. The array measures 26456 (H) × 15072 (V) pixels at 3.9µm pitch. The sensor normally operates in still mode with global reset of all pixels, but can also be configured in video rolling-shutter mode. The array readout is addressed by a single physical row at a time with columns split between top and bottom of the pixel array. The column circuitry and row drivers are controlled by their corresponding logic control block in the two corners, each having its own programmable register space impacting only that sensor side. The column readout consists of the column bias and test circuit, a programmable-gain amplifier (PGA), and two sets of sample-and-hold capacitor banks (S&H) for odd-and-even row ping-pong operation. The pixel signals are then fed directly into the column single-slope ramp ADCs. Their ramp signal is generated by a programmable switched-capacitor-based circuit in the power supply & bias control block, resulting in a clock-frequency-dependent slope covering the required ADC range. Readout of the SRAM data is organized in 24 blocks for the effective pixels. The process technology is from ST Microelectronics with 90nm front-end and 65nm Cu back-end technology. Since the sensor size largely exceeds the reticle size, 2D stitching was developed for this technology. The non-uniformity of the shutter release is optimized through fast signal repetition in the vertical direction from the logic block where shutter control is generated, as well as by row driver slope control and control signal sizing to make the horizontal delay within the pixel array as uniform as possible. This results in global shutter reset uniformity better than 2.5µs over the full pixel array.

Figure 6.3.2 shows the timing diagram of 3 consecutive pixel row readouts. Similar to high-frame-rate sensors, we introduce pipelining of three processes: pixel row access, A-to-D conversion, and SRAM readout. The sizing of the metal lines in the pixel array is the result of the trade-off in settling speed, column voltage swing, QE and angular response. With the 2 available metal layers, we manage to keep the voltage droop on the column line low enough for more than 1.4V swing with sufficient settling in the 67µs line period. The ADC is clocked at 150MHz. On-chip counting ramp A-to-D converters are used, operating with a dual counter scheme per column. These two counters operate at opposite clock edges, in opposite directions and at different periods in the conversion cycle. This scheme doubles the conversion speed compared to earlier similar implementations [2] because both clock edges are used in the conversion process. It also ensures a continuous, signal-independent current consumption during the entire A-to-D conversion avoiding any signal-dependent droops or reference settling issues that could cause row banding errors. This implementation is similar to the earlier reported design [3]. However, counter and SRAM circuitry are split. The comparator output is fed into 15b counters. When the A-to-D conversion is finished, the counter data is written serially into the 19b-wide SRAM with some optional inline correction operations for horizontal droop calibration.

Figure 6.3.3 gives a detailed view of the signal path. The total effective pixel array consists of 6 (H) × 3 (V) repetition of the 4352 (H) × 5000 (V) pixels stitch block. The data readout is further divided in 2 channels and therefore performed on 1088-column-wide blocks. The distribution of the data outputs over the full length of the sensor reduces the length of and data rate on the multiplexing bus and spreads the power consumption evenly at the sensor sides. It also enables the repeatability for and scalability offered by the stitching. All digital parts, including data post-processing (DPP) blocks, subLVDS outputs and power supply connections are thus repeated along the sensor sides. Each DPP block generates its local 11b column address. The left and right optical black (OB) pixel blocks have their own DPP and LVDS channel instances. All data blocks have exactly the same logic and layout. Strapping at the top level configures the behavior of the data block to handle either OB or effective pixels. The incoming 19b raw SRAM data is fed into the processing logic involving programmable digital gain, setting of OB clamped black level and overflow/underflow protection on the ADC data. The reshaped data is sent out, together with synchronization information, to the data outputs. Each pixel row readout is organized in two horizontal timing windows. First, the left and right OB columns are read out to calculate the black offset correction level for each row. Once this clamping algorithm is finished, its calculated value is distributed to the DPP blocks of the effective pixels. Then, the readout of all visible pixels starts, with offset corrected and programmed digital gain, taking at least 1088 pixel periods. The LVDS clock skew is not accurately controlled on-chip, but is compensated in the system by an on-chip supported bit and word alignment protocol.

Figure 6.3.4 shows the measured sensor output temporal dark noise, the linear full-well charge and dynamic range as function of the analog gain set in the PGA. Note that since the analog gain is set with a capacitor ratio, some gain values can be set with multiple register settings. In this case, the scenario with the highest total capacitance is preferred because of the lower bandwidth and resulting better noise performance. With a pixel conversion gain of 45µV/e^-, the pixel noise contribution seen at highest PGA settings (≥4×) is 2e^- rms. The linear dynamic range exceeds 78dB at PGA 1×, and remains above 71dB at PGA 4×. OB clamping reduces the row noise to 0.6 and 0.32e^- rms at these respective PGA gains.

The sensor characteristics are summarized in Fig. 6.3.5, including a comparison with the CCD in [1]. The sensor has an effective resolution of 391Mpixels and maximum frame rate of 1fps. The temporal dark read noise is 3.7e^- rms (PGA gain 1×). Despite the reduced pixel pitch of 3.9µm, the linear saturation signal of 31.5ke^- is slightly higher. This results in a linear dynamic range exceeding 78dB, compared to 67dB for the CCD, mainly due to the almost 4× read noise reduction. Our panchromatic sensor also has nearly twice as high quantum efficiency. The advantage of increased dynamic range enables to reduce the effect of shadows near tall buildings or from clouds. The power consumption is kept as stable as possible during sensor operation and therefore is not fully optimized for lowest average supply current. The sensor consumes approximately 1750mW during full resolution image capture at 14b, of which nearly 30 % is consumed through the 1.2V digital core supply.

Figure 6.3.6 shows a reproduced full-resolution image taken during first test flights by our customer at a flight altitude of about 1200m. The color information originates from 4 smaller-resolution R/G/B/NIR CCD sensors (3.1 PAN/color resolution) in the system. The PAN GSD at this altitude is 5cm with a total swath width of about 1300m. The magnified excerpts show that, besides the benefits stated above, the CMOS sensor has excellent anti-blooming and no smear from highly reflective and over-saturated scene objects. The photograph of the 391Mpixel sensor is shown in Fig. 6.3.7. The diagonal length of the active pixel area is 117.45mm. The total number of sensor IO pads is 664, reduced to 191 pins at package level.

Acknowledgements:
This sensor development was funded by Leica Geosystems, a Hexagon company. We thank their team in Aalen, Germany, for the collaboration and support, as well as the complete Imaging Division and Technology R&D center team at the ST Microelectronics wafer fab in Crolles, France.

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[1] J. Bosiers, et al., "Recent Developments on Large-Area CCDs for Professional Applications," *Int. Image Sensor Workshop (IISW)*, June 2015.
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[3] G. Meynants, et al., "24 MPixel 36 x 24 mm² 14 bit Image Sensor in 110/90 nm CMOS Technology," *Int. Image Sensor Workshop (IISW)*, June 2013.

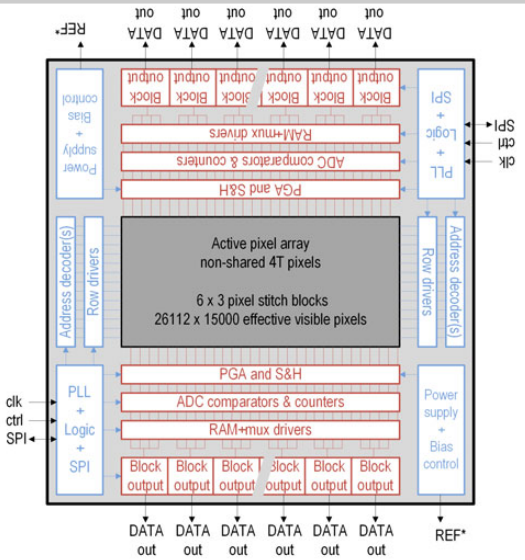

Figure 6.3.1: Overall architecture of the 391Mpixel CMOS sensor.

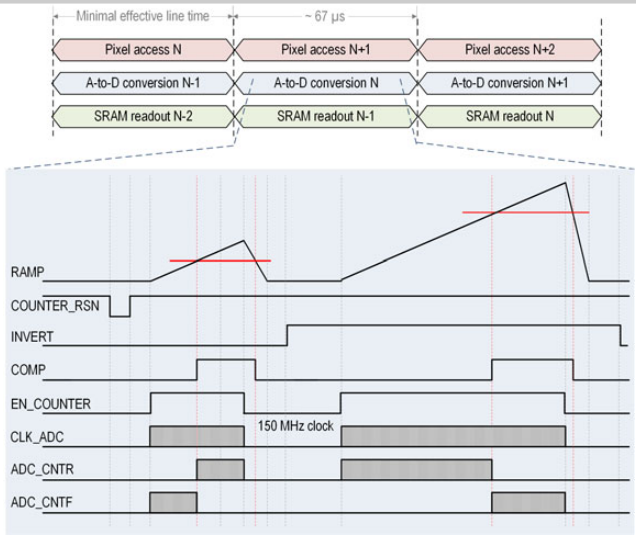

Figure 6.3.2: Pipelined timing diagram and ADC operation principle with dual counters.

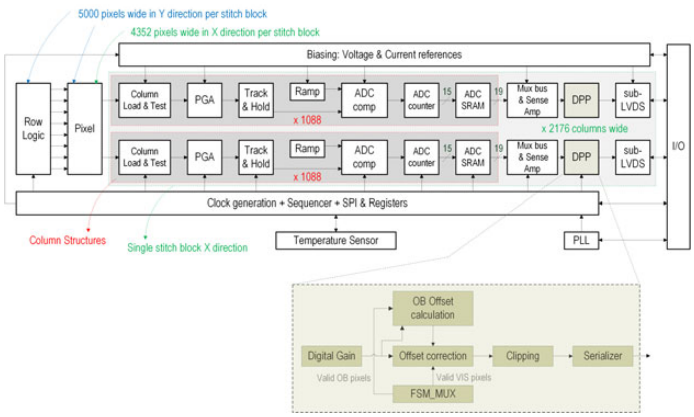

Figure 6.3.3: Signal datapath.

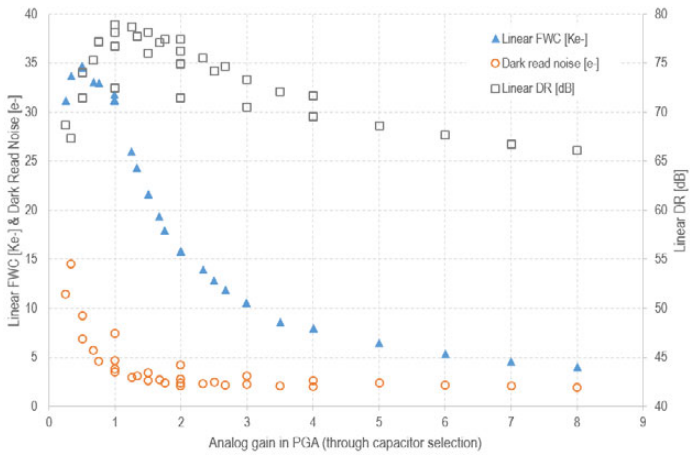

Figure 6.3.4: Overview of measurements of Dark Read Noise, Linear FWC and Dynamic Range as function of the analog gain setting in the PGA.

	This work		[1]
Technology	ST Microelectronics 90 nm FE, 65 nm BE, 1P4M, 12 inch wafers		CCD
Supply voltage	3.5 / 3.3 / 2.7 / 1.8 / 1.2 V (externally supplied)		
Pixel size	3.9 µm pitch		5.6 µm pitch
Number of pixels	Total	26456 (H) x 15072 (V)	
	Effective	26112 (H) x 15000 (V)	17216 (H) x 14656 (V)
Active area	101.84 (H) mm x 58.50 (V) mm		96 (H) mm x 82 (V) mm
Chip size	105.18 (H) mm x 65.63 (V) mm, 6 gross dies per wafer		
Frame rate	1 fps		1 fps
Clock input	6-12 MHz		27 MHz
Output data	Type	24 effective data + 4 OB + 2 clock LVDS lanes @ 300 Mbps (DDR)	16 analog channels
	Total Rate	5.474 Gbps from effective pixels	
Number of IO pads	664 sensor pads, 191 package pins		
ADC	14-bit SS ADC with dual counters, 150 MHz clock		N/A
Pixel type	4T non-shared		
Linear Full Well Capacity	31.5 Kelectrons @ PGA x1 and 1 % linearity		~ 31.3 Kelectrons (calc.)
Conversion gain	45 µV/e-		
Temporal noise	3.7 e- @ PGA x1, 2 e- @ PGA x4		14 e-
Dynamic range	> 78 dB @ PGA x1, > 71 dB @ PGA x4		67 dB
Fixed pattern noise	8.8 e- @ PGA x1, short exposure time, w/o column calibration procedure		
Photo-response non-uniformity	1 % rms, stitch difference 0.5 %		
QE	75 % peak (mono, no CFA, with micro lens)		35-40 % peak (mono) (est.)
Angular response	> 80 % @ 18 °		
Dark current	95 e-/s @ 60 °C		
Power consumption	1750 mW @ 1 fps full resolution 14-bit		

Figure 6.3.5: Performance table and comparison to CCD in [1].

Figure 6.3.6: Full-resolution image (left) and two magnified image excerpts (right) (4ms exposure time, f/5.6).

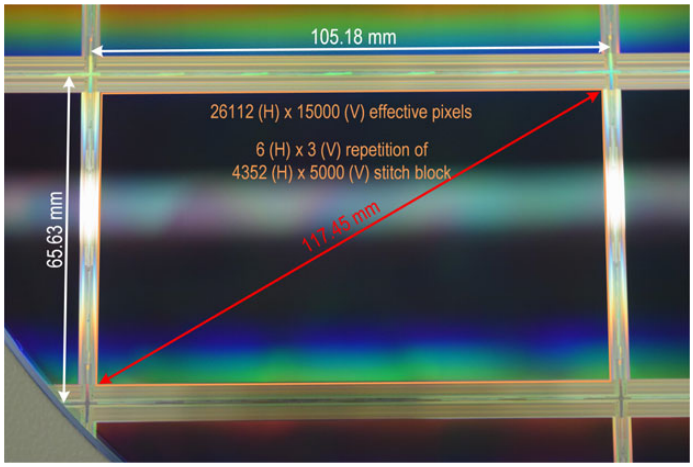

Figure 6.3.7: Chip photograph at wafer level (12-inch wafer, 6 GDPW).

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6.4 An APS-H-Size 250Mpixel CMOS Image Sensor Using Column Single-Slope ADCs with Dual-Gain Amplifiers

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Recently, there has been strong demand for high-resolution CMOS image sensors (large number of pixels) in the fields of security, science, and other specialized areas [1,2]. One of the major issues in realizing high-resolution image sensors is to speed up signal readout. For high-speed signal readout, it is necessary to accelerate pixel readout, AD conversion in column circuits, horizontal data output from column memories, and digital data output from the chip. Single-slope ADCs (SS-ADC) are the most common architecture in commercialized CMOS image sensors; increasing their counting clock frequency up to 2.376GHz [3] and using multiple ramp signals [4] can shorten the AD conversion period. However, the former has difficulty in maintaining the clock quality and suppressing power dissipation due to the high clock frequency, and the latter has difficulty in controlling the uniformity and the quality of the multiple ramp signals. Another significant issue is power consumption. Rise of power consumption with increase in number of columns results in non-uniformity of power supply to the column circuits due to IR drops. It may give rise to degradation of image quality such as fixed pattern noise, etc.

This paper presents an APS-H-sized 250Mpixel CMOS image sensor implemented with column SS-ADCs with dual-gain amplifiers (SSDG-ADC) to shorten the AD conversion period and widen the dynamic range without a rise in power consumption. In the SSDG-ADC, the gain of the column amplifier that is placed in front of the comparator is set to high gain (4×) when a pixel signal level is lower than a certain threshold level (roughly 1/4 of the pixel signal range) to reduce random noise (RN). To avoid exceeding the amplifier output range, the gain is set down to low gain (1×) when the pixel signal level is higher than the threshold. Since RN is suppressed while keeping the pixel signal range, the dynamic range is wider than for a SS-ADC. The comparator then converts the signal to digital data using a ramp signal of 4× steeper slope than for a SS-ADC. Because of the steeper ramp signal, the AD conversion period is shortened to about 1/4 that of a SS-ADC. As a result, the 250Mpixel sensor with 12b SSDG-ADC performs in about 75% shorter AD conversion period and 6dB wider dynamic range than a SS-ADC, without increasing power consumption.

The block diagram of the sensor is shown in Fig. 6.4.1. The sensor is composed of a pixel array, column readout circuits, column memories, signal processors and Scalable Low-Voltage Signaling (SLVS) interfaces. The pixel array has 19,712(H) × 12,752(V) = 251.4Mpixels and the pixel pitch is 1.5μm. The column readout circuits and memories are configured on both upper and lower sides of the pixel array. Ramp generators are connected to the column readout circuits of each side for supplying the ramp signal. To reduce the power consumption of the column memories, a common counter outputs multiple count signals with gray-code to the column memories on each side with 810MHz count frequency, and the count signals are latched at the column memories. To accelerate the circuits, the pixels and column circuits are driven by the pulse drivers located on the both right and left sides. The signal processor decodes the gray-coded data to binary and performs a digital Correlated Double Sampling (CDS). The processor also does a compensation process to mitigate the image degradation caused by SSDG-ADC.

The column circuit diagram for the SSDG-ADC is described in Fig. 6.4.2. Amplifier gain can be set either high (4×) or low (1×) through switch SW1 controlled by the Judge flag from the limiting circuit. When the amplifier output V_{ampo} is larger than the threshold level determined by V_{jdg}, the limiting circuit sets the Judge flag (Judge = 1) with clipping V_{ampo} to prevent the saturation of the amplifier by PMOS transistor M2. Since most of the current consumed by the limiting circuit is supplied from load PMOS transistor M1 of the amplifier, the increase in power consumption from adding the limiting circuit is negligible. The Judge flag is held at the column memories.

A timing chart of the SSDG-ADC is presented in Fig. 6.4.3. After clamping the pixel reset level at the amplifier with the gain of 4×, the first AD conversion is done (N-AD). When the pulse Ptx is activated, the pixel output signal V_{pixo} and V_{ampo} change according to the amount of electrical charges accumulated in a photodiode. In case of signal level higher than the threshold, V_{ampo} is limited by the limiting circuit before the amplifier is saturated, and the Judge flag is set (Judge = 1) and held at the memory. The gain is set down to 1× by the feedback of the Judge flag. In the lower signal level case, V_{ampo} is not limited, 4× gain is kept, and Judge = 0. Then, the second AD conversion (S-AD) is conducted with each gain set according to its signal level. The results of the AD conversions with the Judge value are transferred to the signal processor. At the signal processor, if Judge = 0, only the digital CDS is conducted, and if Judge = 1, the data after the digital CDS is multiplied by 4 in order to equalize the total conversion gain between the high-gain and the low-gain signals.

Linearity errors may occur when the results of the high-gain and the low-gain signals are connected to each other at the threshold level. The main factors leading to the error are relative gain deviation and offset deviation between the column amplifiers. Since large linearity errors may be perceived in an image, a compensation process is required to reduce the errors. In the process, the gain coefficient α and the offset coefficient β are obtained using the following steps before the signal readout for image capturing. First, two input signal levels A_H and A_L are converted by SS-ADC to B_{H1} and B_{L1} at gain 1×, and B_{H4} and B_{L4} at gain 4×, respectively. Second, α and β are given by:

$$\alpha = (B_{H4} - B_{L4}) / (4 \times (B_{H1} - B_{L1})) \text{ and } \beta = B_{L4} - 4 \times B_{L1} \times \alpha.$$

In terms of β, the upper and lower column readout circuits are divided into 8 blocks each, and β of each block is assigned individually. During the signal readout for image capturing, converted data that has Judge = 1 is compensated by the calculation according to the following formula with the digital CDS process at the signal processor,

$$4 \times (S\text{-}N) \times \alpha + \beta,$$

where S and N are results of S-AD and N-AD, respectively.

Figure 6.4.4 shows measurement results of the linearity errors over all columns before and after the compensation and input/output characteristics of the 9,800th column. The result of raw linearity errors is roughly -135 LSB on average and has a shading pattern with about 20 LSB peak-to-peak. This level of errors may cause noticeable image degradation. On the other hand, the linearity errors after the compensation are kept almost within the range of ±5 LSB. The captured image and zoomed views before and after the compensation are shown in Fig. 6.4.5. The linearity errors are recognized as a reddish belt-like pattern on the egg surface in the upper zoomed image (before compensation). That pattern at the same place in the lower zoomed image is suppressed to an unrecognizable level and the compensation effect is verified.

Figure 6.4.6 summarizes the specifications of the sensor. The chip is fabricated using 0.13μm 1P4M CMOS process and the power supply voltages are 3.3 and 1.2V. The maximum frame rate of the sensor is 5fps at full pixel readout, 24fps at 8k4k, and 48fps at 4k2k. Power consumption is 1.97W at 5fps full-pixel readout with 12b SSDG-ADC. The dynamic range for SSDG-ADC is 66.7dB and is 6dB wider than SS-ADC. The chip microphotograph is shown in Fig. 6.4.7.

Acknowledgement:
The authors are deeply grateful to the members of Device Technology Development Headquarters, Canon Inc. for their support of this work.

References:

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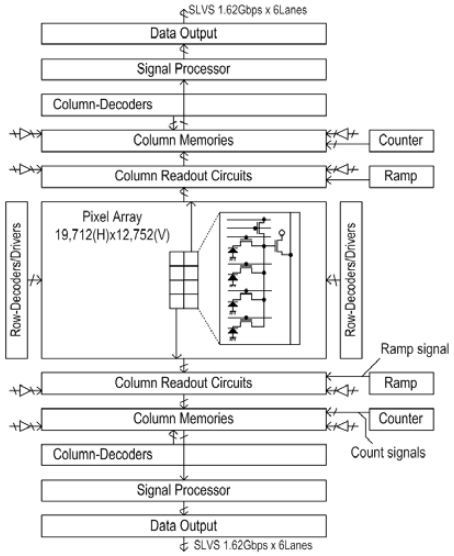

Figure 6.4.1: Block diagram of the sensor chip.

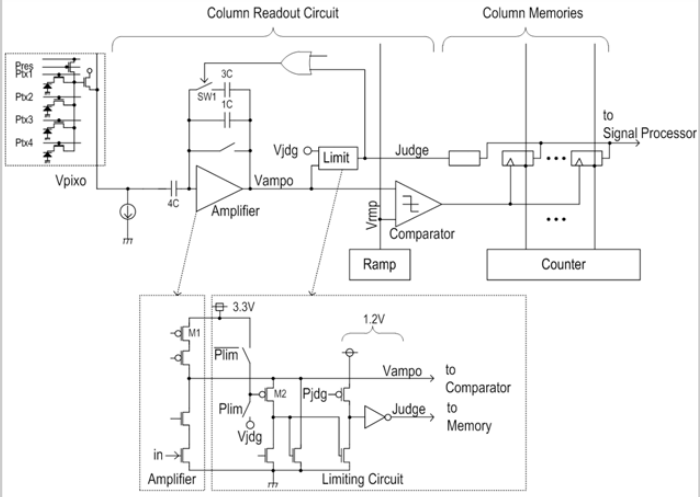

Figure 6.4.2: Circuit diagram of the column circuit.

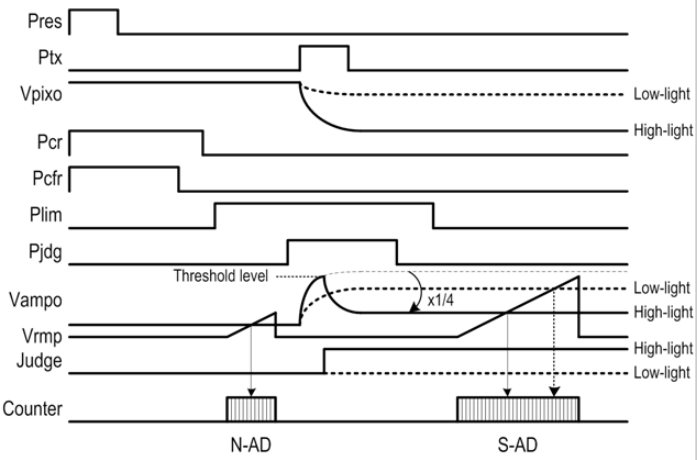

Figure 6.4.3: Timing chart of SSDG-ADC.

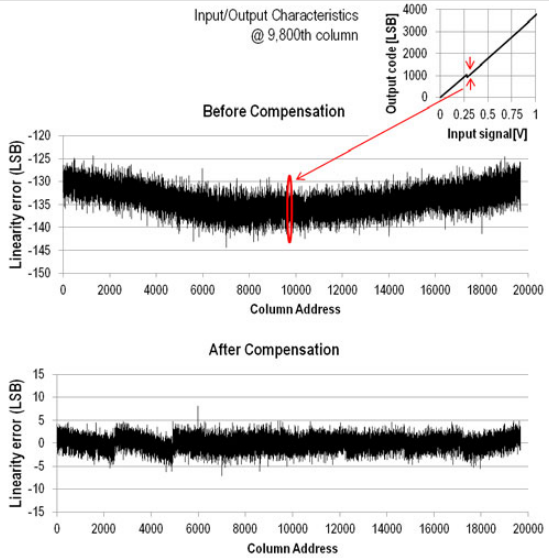

Figure 6.4.4: Measured linearity errors.

Figure 6.4.5: Captured image and zoomed views.

Process		0.13 µm 1P4M CMOS
Power supply		3.3 V / 1.2 V
Die size		32.84 mm x 25.84 mm
Number of pixels	Total	19,712(H) x 12,752(V) = 251.4M pixels
	Valid	19,568(H) x 12,588(V) = 246.3M pixels
Pixel size		1.5 µm x 1.5 µm
Maximum frame rate	Full pixel	5 fps
	8k4k	24 fps
	4k2k	48 fps
Power consumption		1.97 W
Frequency of ADC count clock		810M Hz
Sensitivity		4,100 e-/lx/sec
Full Well Capacity		7550 e-
Dark Random noise	SS-ADC	7.1 e^-_{rms}
	SSDG-ADC	3.5 e^-_{rms}
Dynamic range	SS-ADC	60.5 dB
	SSDG-ADC	66.7 dB
Dark Current		7 e-/sec @60°c
Conversion Gain		91 µV/e-

Figure 6.4.6: Chip specifications.

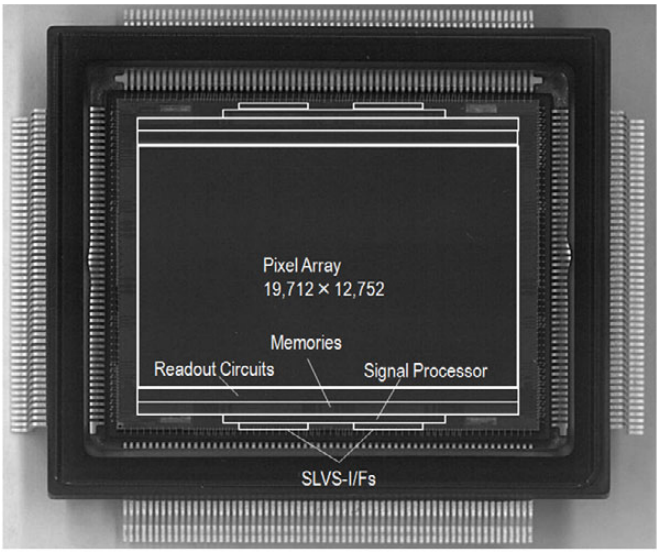

Figure 6.4.7: Chip microphotograph.

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6.5 A 64×64-Pixel Digital Silicon Photomultiplier Direct ToF Sensor with 100MPhotons/s/pixel Background Rejection and Imaging/Altimeter Mode with 0.14% Precision up to 6km for Spacecraft Navigation and Landing

Matteo Perenzoni, Daniele Perenzoni, David Stoppa

Fondazione Bruno Kessler, Trento, Italy

Recent technology surveys identified flash light detection and ranging technology as the best choice for the navigation and landing of spacecrafts in extraplanetary missions, working from single-point altimeter to range-imaging camera mode. Among all available technologies for a 2D array of direct time-of-flight (DTOF) pixels, CMOS single-photon avalanche diodes (SPADs) represent the ideal candidate due to their rugged design and electronics integration. However, state-of-the-art SPAD imagers are not designed for operation over a wide variety of scenarios, including variable background light, very long to short range, or fast relative movement.

A typical DTOF imager consists of a per-pixel time-to-digital converter (TDC) capturing the timestamp of the first detected photon [1]. However, in presence of background light, high dark-count rate (DCR), or long observation time, the probability of catching an unwanted event instead of the light echo becomes very high and the creation of pixel timing histograms is extremely inefficient. Delta-sigma operation as a method of filtering out the illumination signal [2] or very-low-DCR SPAD devices [3] mitigate the issue, but the light echo photons are still not identified. This is addressed in [4] by means of detection of photons occurring closely in time, but the required circuitry size does not allow implementation of this scheme in a 2D array structure, as needed for fast-moving spacecraft applications. Time gating is also a mitigating solution [5].

The proposed image sensor implements a pixel based on a digital silicon-photomultiplier (dSiPM), i.e., a set of SPADs providing on a single output a stream of short pulses corresponding to each avalanche, coupled to a smart triggering logic for concurrent-event detection, allowing uniquely correlated photons' time-stamping and counting.

The pixel architecture is sketched in Fig. 6.5.1: 8 SPADs with NMOS quenching and inverter front-end are combined together in a dSiPM, using monostables followed by an OR tree. The monostable pulse width determines the lower bound below which the events are merged and become undistinguishable. The circuit shown in Fig. 6.5.1 (inset), differently from the one used in [4], produces minimum-size pulses ensuring complete settling in all process corners thanks to the feedback loop, in a very small footprint. The OR tree is composed of alternating NAND and NOR gates for area saving and its output can be inhibited by a gating signal. The dSiPM output is analyzed by smart triggering logic, detailed in Fig. 6.5.1 (inset), which produces the stimulus for the TDC and counter. The TDC has two operating modes: (a) one for short range where an 8b ripple counter coarsely counts the global clock cycles and a ring-oscillator-based TDC finely measures the time from the event to the first clock edge after validation, and (b) one for long range where the 7b and 8b counters are chained and measure the number of clock cycles until the event detection.

The overall architecture of the 64×64 imager shown in Fig. 6.5.2 reveals a compact peripheral circuit, with decoders and serializers for byte-serialized 3×8-bit digital output. An additional row of pixels acting only as DCR monitors, with dSiPM output directly fed into an 8b counter increases testability and monitoring of SPAD DCR. Eventually, a PLL with a TDC replica is used to lock the pixel TDCs to a stable reference voltage. The imager operation can be described with the waveforms of Fig. 6.5.2: all pixels are reset and clocked simultaneously, and the pulses are optionally inhibited by the GATE signal for an initial period so as to reduce potential atmospheric and dust backscattering. Independent for each pixel, the dSiPM pulses activate the beginning of an asynchronous observation window, represented by the TRIG signal. The fine-resolution TDC is immediately started, while at each subsequent dSiPM pulse, the smart triggering logic compares the configured N_{ph} value to the number of pulses falling into the TRIG pulse width. If the threshold is reached, a validation signal TRIGOK is produced: the logic stops the TDC on the first global clock edge and inhibits the pixel operation until readout and reset. Otherwise, at the end of the observation window, TRIG returns to zero and a short RESINT pulse resets TDC and counter for subsequent triggers.

The chip, shown in the micrograph of Fig. 6.5.7, is fabricated in standard 0.15μm CMOS: SPADs are implemented with pplus on nwell diodes using non-minimum guardrings, a choice guaranteeing low crosstalk. In order to optimize the fill-factor, pixels are mirrored, sharing the deep nwell implant, and obtaining a pitch of 60mm with a fill-factor of 26.5%.

The final target system is schematically shown on the left of Fig. 6.5.3: the imaging mode employs flood illumination of the scene through a high-power laser at a wavelength of 532nm and images are acquired so as to characterize the surface before spacecraft landing. In the navigation phase, at a large distance from the surface, the laser is focused to implement the altimeter mode, where the sensor sees a spot of about 2×2 pixels in size. In both cases, a narrowband filter removes part of the background light. In order to reproduce this condition, a setup involving a delayed low-power laser at 470nm wavelength (where used SPADs have similar quantum efficiency with respect to 532nm) and a set of neutral-density filters with an additional background light source is tuned based on the final system specifications. The calculated power density, shown in the graph of Fig. 6.5.3, is employed in the following measurements.

Due to the high relative speed of the spacecraft, a measurement is composed of only 250 acquisitions, resulting in a very sparse histogram. Although very complex algorithms can be used, Fig. 6.5.4 shows the simple benchmarking method adopted, which provides a baseline for comparison of the sensor configurations: the histogram is first filtered with a moving average, which lowers isolated events, and then identifies the maximum. Its position in the histogram is then the center of a weighted average that takes into account the width of the laser echo. The rightmost part of Fig. 6.5.4 shows the images obtained with a distance measurement of 250 acquisitions, with an emulated echo at ≈164m, with different N_{ph} and background: it can be noted that N_{ph} = 1 fails dramatically with the 100Mph/s/pixel background, while correlation of 2 or 3 photons guarantees reliable operation. The smaller spot size for increasing N_{ph} is due to the Gaussian distribution of the intensity, lowering the probability of having 2 or 3 correlated photons at the periphery.

By applying the calculated attenuations and delays, the reliability of the measurement can be evaluated in almost the whole expected range: Fig. 6.5.5 reports the results of 10 distance measurements at 250 acquisitions, on a 8×8-pixel region at the center of the laser spot, in imaging and altimeter modes. The data processing is then applied to each single pixel in imaging mode, while in altimeter mode a 2×2 cluster is considered: when the algorithm did not obtain a maximum in the histogram, the measurement was discarded. The average precision and the accuracy of all valid measurements for each pixel or cluster is computed and shows reliable operation up to the specification of the operating modes, although with reduced measurement efficiency at the higher end of the range for high background conditions. In the altimeter mode with background, the whole range can be covered by setting N_{ph} = 3.

The power consumption of the digital electronics amounts to 47.7mW and is mainly determined by the distribution of the clock and the TDC counters, while the SPAD high-voltage supply consumes 45.8mW in typical operation, and depends on the illumination conditions. The chip performance is summarized in Fig. 6.5.6.

Acknowledgments:
Thanks to V. Mitev, J. Haesler, C. Pache, T. Herr and A. Pollini for the conception of multimode operation. The work is carried out under a programme funded by the European Space Agency. (Disclaimer: the view expressed herein can in no way be taken to reflect the official opinion of the European Space Agency)

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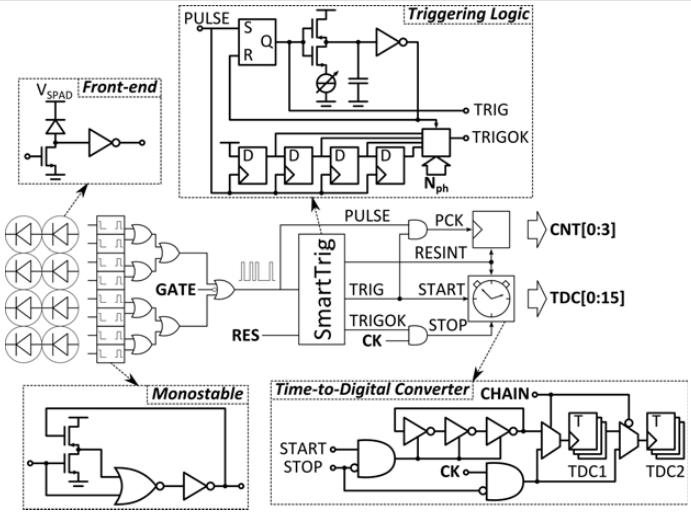

Figure 6.5.1: Pixel high-level schematic with detailed insets for the main blocks: SPAD front-end, monostable, smart triggering logic, time-to-digital converter.

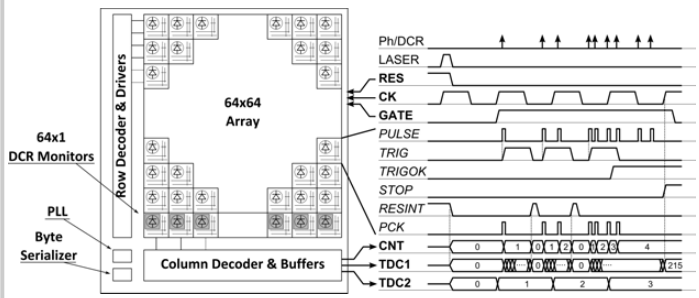

Figure 6.5.2: Architecture of the imager and waveforms describing the sensor operation: in bold, externally driven/readable global signals, while the italic names are pixel internal signals. The example is given for 3 correlated photons in the short-range operating mode.

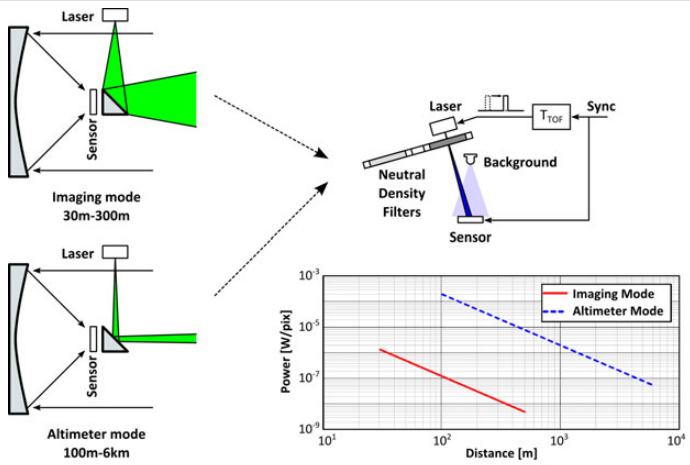

Figure 6.5.3: Characterization of the sensor: the final system configuration is shown, with the two operating modes, and the laboratory setup used to reproduce the same power density and pulse delay conditions. The graph shows the power density on the pixel for a 50% reflectivity target.

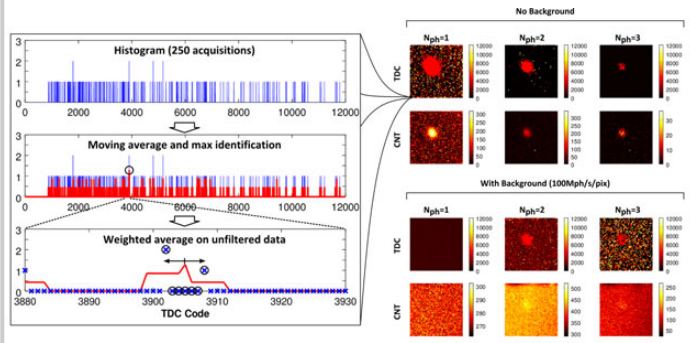

Figure 6.5.4: Sensor data acquisition and processing in imaging mode. In the inset, a pictorial description of the algorithm applied on 250 acquisitions. Images show the resulting TDC and intensity of the laser spot, with and without strong background of 100Mph/pixel.

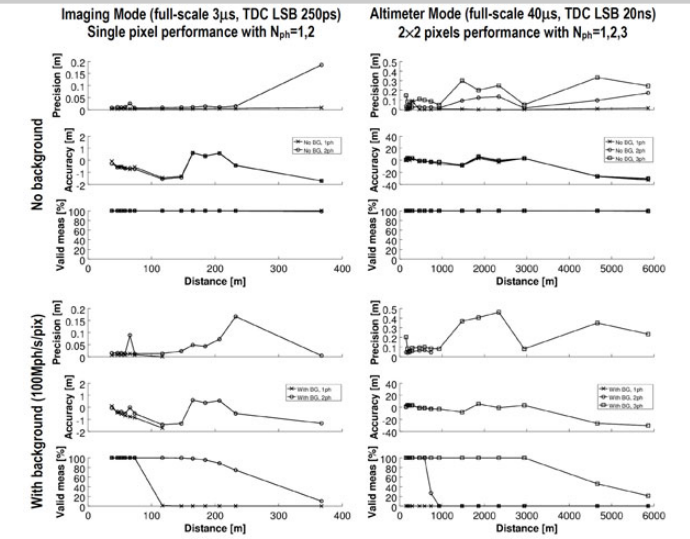

Figure 6.5.5: Results of range measurement with the emulated laser attenuation and delay for a 50% reflectivity diffusive target.

Parameter	Note	Value	Unit
Chip characteristics			
Array resolution		64×64	
Technology		CMOS 150nm 6M	
Chip size		4.4×4.4	mm^2
Pixel pitch		60	µm
Pixel fill-factor		26.5	%
SPAD operating voltage	V_{exc}=3.0V	21.8	V
SPAD median DCR	V_{exc}=3.0V	6.8	kHz
TDC resolution	Imaging mode Altimeter mode	250 20	ps ns
TDC depth	Imaging mode Altimeter mode	16 15	bit bit
Max frame rate (1 point)		1920	fps
Frame rate (250 points)	Imaging mode Altimeter mode	7.68 7.16	fps fps
Power consumption	Digital 1.8V, 3.3V SPAD 21.8V	47.7 45.8	mW mW
Emulated distance measurement performance			
Distance range	Imaging mode Altimeter mode	367 5862	m m
Precision (σ)	Imaging mode Altimeter mode 	<0.2 <0.13 <0.5 <0.14	m % m %
Accuracy	Imaging mode Altimeter mode 	<1.5 <0.37 <35 <1.9	m % m %
Background flux		100	Mph/s/pix

Figure 6.5.6: Chip performance summary table.

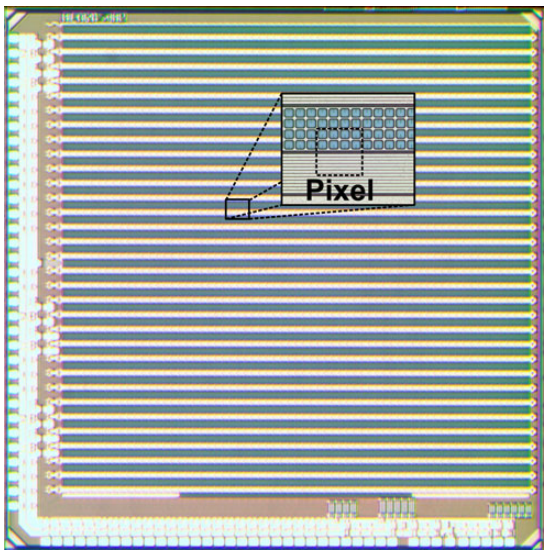

Figure 6.5.7: Chip micrograph.

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6.6 A 1280×720 Single-Photon-Detecting Image Sensor with 100dB Dynamic Range Using a Sensitivity-Boosting Technique

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Continuous improvements in sensitivity have opened up applications for image sensors such as camcorders, digital still cameras, mobile phones, and surveillance cameras. Even though leading-edge image sensors have reached the noise floor of a few electrons [1,2], a thrust towards darker levels still continues down to an illumination level equivalent to being under a crescent moon (i.e., 10^{-2} down to 10^{-4} lux). This requires single-photon detection with typical digital cameras pixel size, i.e., 1.5 to 5μm. Although huge-size pixel [3] or single-photon avalanche photodiode (SPAD) based image sensors [4] have been presented for such a purpose, in general, both have to pay area and dark current penalties. Thus, an image sensor capable of both single-photon detection and normal imaging providing us with a high dynamic range is a huge technological challenge.

In this paper, we report a sensitivity-boosting technique that incorporates dual operation modes, i.e., normal (NL) and high-sensitivity (HS), into one photodiode in each 3.8μm pixel. In the NL mode, the photodiode converts multiple photons to electrons and accumulates them, in a similar way to conventional photodiodes [5]. In the HS mode, single-photon detection is achieved by avalanche multiplication of one photo-electron, typically with a gain larger than 10^5, while keeping the dark count rate as low as 0.1cps. The technique is enabled by introducing a photodiode potential design that realizes perfect electric field confinement in the vertical direction; this eliminates local electric field concentration and separates the avalanche region from dark-current-generation regions. The dynamic range of the present sensor can be improved to 100dB by synthesizing images captured under these two modes. Although conventional image sensors need infrared illumination to image such a dark environment [6], the reported image sensor enables true color imaging without infrared illumination. Under the 10^{-4} lux condition, the photon flux irradiated on each pixel is about 1 photon/1.25s using a lens with an F-number of 1.4. Therefore, we establish the validity of single-photon imaging at a frame rate of 30fps.

The pixel is developed based on a backside-illumination structure with a pinned photodiode, in which an abrupt p-n junction acting both as an NL and an avalanche photodiode is added between a p^- region and an n region, as shown in Fig. 6.6.1. We note that the electric field across the p-n junction is entirely parallel in the vertical direction, along which photo-generated carriers are transferred. This is in high contrast to typical SPAD-based pixels that suffer from electric field crowding due to coexistence of lateral and vertical fields. The vertical field strength of the present photodiode is controlled by the potential of a surface p^+ layer. During the NL mode, a DC bias of V_{P+} is applied to the p^+ layer and the electric field is lower than the critical field for avalanche multiplication. Photo-generated electrons in the p^- region run through the p-n junction and are stored in the n region. During the HS mode, on the other hand, a DC bias of V_{APD} is applied to the p^+ layer and the electric filed is elevated to be higher than the critical field. Photo-generated electrons are accelerated by the field and eventually multiplied by impact ionization.

Figure 6.6.2 shows the DC-bias dependence of the avalanche multiplication ratio and the dark count rate. Typical DC bias of the HS mode, V_{APD}, is determined to be -23.3V, since a ratio of 10^5 is sufficient to overcome the readout noise. With these bias conditions, the electric fields across the p-n junction during the NL mode and the HS mode are calculated to be 4.0×10^7V/m and 4.4×10^7V/m, respectively. In order to completely switch from the NL mode to the HS mode (or vice versa) within 1ms, the voltage swing between the two modes, which charge and discharge a total capacitance of 1.3nF, is set to be 2.0V, i.e., V_{P+} is -21.3V and V_{APD} is -23.3V. The switching time of 1ms is about one order of magnitude shorter than usual exposure period. Thus, alternating the two operation modes enables wide operational range extending to dark conditions at a typical frame rate of 15 fps.

We carefully designed the potential profile inside the photodiode where the electric field is parallel and uniform along the vertical (i.e., optical) axis so as to not increase the dark current due to the convergence of the electric field. The effectiveness of this design is verified by the photodiode's I-V performance shown in Fig. 6.6.2 where, with respect to the applied voltage, the behavior of the increase of the dark count rate (curve A) significantly deviates from that of the avalanche multiplication ratio (curve B). This fact indicates that the added p-n junction structure is not the major origin of noise electrons. Thus, the present photodiode design enables enhancement of only the signal electrons while keeping noise electrons in the low level, i.e., as low as 0.1cps at -23.3V.

A block diagram of the image sensor is shown in Fig. 6.6.3. The pixel circuit, which is completely isolated from the photodiode as shown in Fig. 6.6.1, has a conventional 4-transistor configuration. The sensor comprises a 1280×720-pixel array with a vertical shift resistor, a correlated double sampling, a level-shift circuit, and a horizontal shift resistor. An external control IC controls the voltage connected to the p^+-type layer of the photon detective region. To adjust the sensitivity of the photon detective region corresponding to the object illuminance, it is set to a voltage of V_{P+} or $V_{APD.}$ With the NL mode, the sensor gives an analog output in proportion to the amount of incident light. While with the HS mode, it gives rise to binary output only dependent on the presence of a single photon.

The measured sensitivity performance of the image sensor is shown in Fig. 6.6.4. In the NL mode, a highly linear output in proportion to the number of incident photons, is confirmed as represented by the name of the mode, the "normal" photodiode operation. On switching to the HS mode, one photo-electron generated by one photon is multiplied up to 10^5 or more electrons by the avalanche effect. The signal output reaches the readout output maximum or the saturation level, giving rise to the binary or the digital readout scheme immune to the analog noise floor. The reproduced images taken by the image sensor with an exposure time of 0.033s are shown in Fig. 6.6.5. The color image in the HS mode demonstrates the effectiveness of the pinned photodiode with the avalanche multiplication. On the other hand, the color image in the NL mode has the same quality as that of a commercially available high sensitivity digital still camera. Thus, the image sensor enables high quality images under both daylight and moonlit conditions or equivalently, a high dynamic range of 100dB. The sensor performances are summarized in Figure 6.6.6.The fabricated image sensor is shown in Fig. 6.6.7.

In conclusion, we have successfully demonstrated a high dynamic range imaging of 100dB from 10^{-4} lux to 10 lux by developing a sensitivity-boosting technique incorporating an avalanche multiplication and the NL mode into one photodiode in each pixel. The sensor is expected to provide natural color vision in dark environments and to open up new applications.

Acknowledgements:
The authors are grateful to Mr. S. Teranishi of University of Hyogo and Shizuoka University for his valuable technical comments. The authors also are grateful to Dr. E. Fujii for his continuous encouragement.

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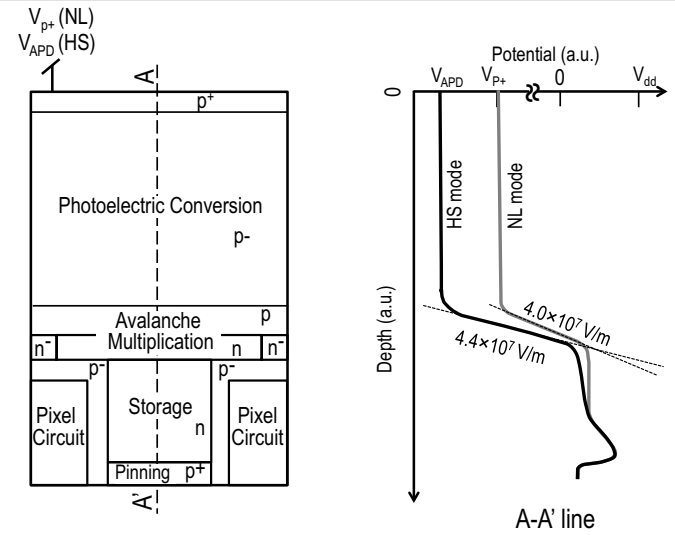

Figure 6.6.1: Schematic view of a dual-mode photodiode and its potential profiles along a A-A f line.

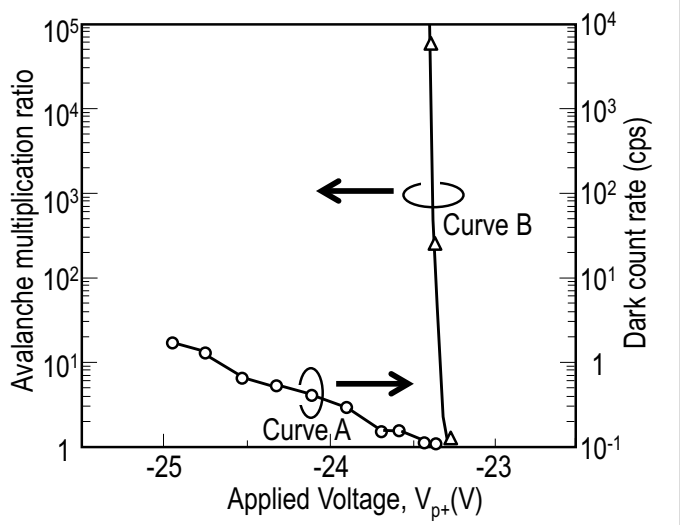

Figure 6.6.2: Applied voltage dependences of avalanche multiplication ratio and dark count rate.

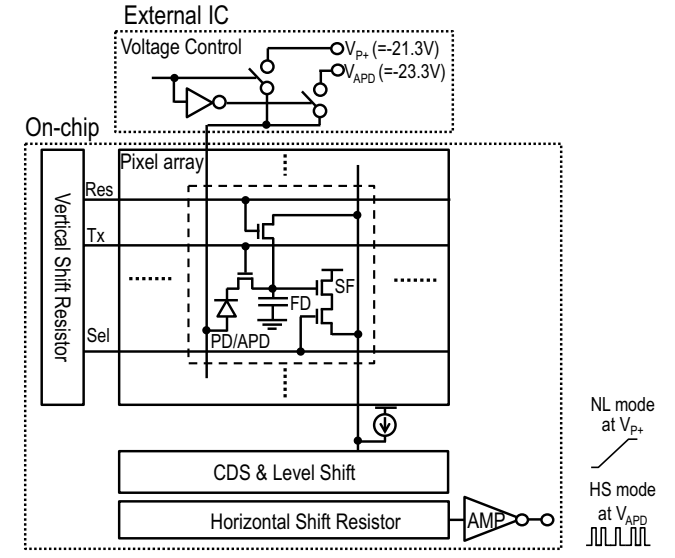

Figure 6.6.3: Block diagram of the image sensor.

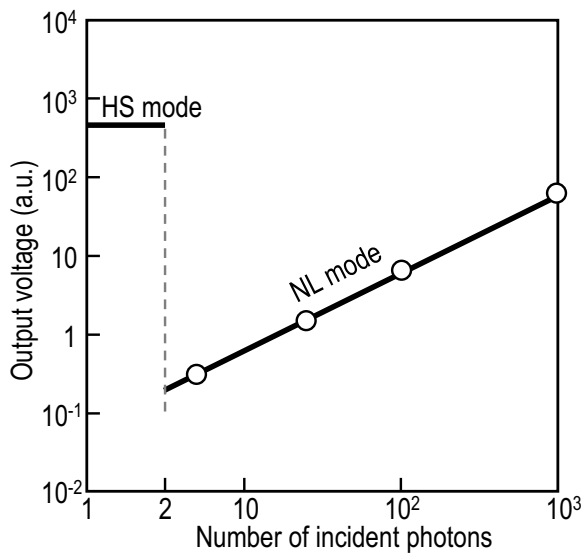

Figure 6.6.4: Sensitivity performance of the image sensor.

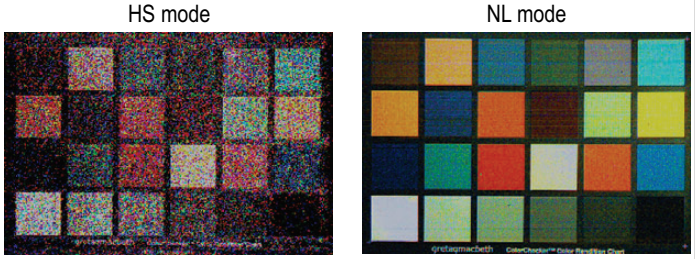

Figure 6.6.5: Reproduced images of 1280 x 760 pixels with an exposure time of 0.033 s.

	This Work		ISSCC 2011 [3]	VLSI 2014 [4]
	NL mode	HS mode		
Pixel size	3.8 μm		160 μm	8 μm
Number of pixels	1280(H) x 720(V)		1280(H) x 1128(V)	320(H) x 240(V)
Process technology	110nm CMOS (1P,4M) Back Side Illumination		0.25μm CMOS (1P,3M) Front Side Illumination	0.13μm CMOS (1P,4M) Front Side Illumination
Supply voltage	3.3 V		NA	NA
Operation voltage of V_{p+}	-21.3 V	-23.3 V	NA	NA
The minimum value of photon detection	3 photons	1 photon	13 photons (Random Noise Floor)	1 photon
Dark characteristic @R.T.	100 nA/m^2	0.1 cps	NA	NA
Dynamic range	60 dB	40 dB	75 dB	52 dB
	100 dB			

Figure 6.6.6: Sensor performances.

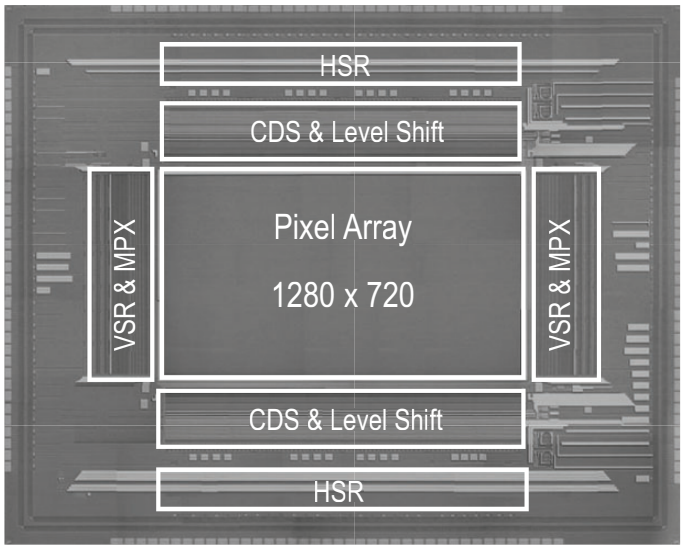

Figure 6.6.7:

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6.7 A 1.2e⁻ Temporal Noise 3D-Stacked CMOS Image Sensor with Comparator-Based Multiple-Sampling PGA

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This paper presents a 1.2e⁻, 3D-stacked CMOS image sensor (CIS) for mobile applications. A key motivation for using a stacked configuration is to minimize the chip area. Also, since numerous components must be integrated into the bottom chip, a scaled 65nm CMOS process is adopted for the bottom chip. The developed CIS features 1.2e⁻ temporal noise with extremely high power efficiency by employing a multiple-sampling (MS) technique. A 2nd-order incremental ΔΣ ADC with inverter-based switched-capacitor integrator realizes the MS technique with low power [1]. However, an exponential number of samples are required to reduce the quantization noise, and conversion speed worsens with higher bit resolution. An extended counting ADC, which is a blend of folding integration and cyclic ADC, attains high resolution with reduced conversion time [2-3]. However, an op-amp with high open-loop gain is required for good linearity and column-to-column matching characteristics, which increases power consumption. Also it is not suitable for scaled CMOS technology. An alternative approach is a single-slope (SS) based MS technique [4], in which two SS-ADCs convert the same pixel signal, and the readout signal is averaged in the digital domain, but the noise improvement is limited to -3dB and the power consumption and area occupation are roughly doubled.

Figure 6.7.1 shows the block diagram of the implemented CIS. 3312×2524 pixels are implemented on the top chip. The bottom chip consists of row drivers/decoders, load transistors, analog MUX, column readouts, a shift register, and other peripheral circuits, where the individual column readouts consist of a PGA and an 11b SS-ADC. Two chips are connected with a Cu-Cu direct bonding. The Cu-Cu bonding is effective for minimizing the chip size compared to TSV-based stacking [4], because it does not set a restriction on the interconnection position and area. In this CIS, the switched-capacitor (SC) integrator is embedded into the PGA, and the gain is determined by the number of integration steps (M). For a large value of M, the MS-PGA achieves low temporal noise. To minimize the power consumption of the PGA, a comparator-based switched-capacitor (CBSC) circuit is used instead of an op-amp-based switched-capacitor (OBSC) circuit. Since the CBSC is less sensitive to supply voltage and intrinsic gain of transistors, it is suitable for low-power design in scaled CMOS. In addition, the column readout employs a 2-channel capacitor bank to enable parallel operation of the PGA and the SS-ADC, which improves the conversion speed. Another feature is a modified SS-ADC to further improve the power efficiency of the column readout. A look-ahead (LA) circuit is implemented inside each column to predict the pixel signal level before the decision time of the static comparator (S-CMP) in the SS-ADC, and to cut unnecessary power consumed by the S-CMP and the counter.

Figure 6.7.2 shows the timing diagram of the MS-PGA. The pipelined operation of the MS-PGA and the SS-ADC effectively increases the number of multiple samples up to 32 by keeping a frame rate of >20fps. Two charge pumps (CPs) composed of SC integrators alternately integrate the pixel signal with two control signals Φ_A and Φ_B, and either capacitor holds the amplified signal to be processed with the SS-ADC, while the other performs signal integration of the next input. The comparator current strongly determines the input-referred noise of the readout and consumes 11μA in each column. The CP current is 1μA, and the total current of the MS-PGA at M=16 is 13μA in each column, including the MS controller. The timing diagram of the LA-SS-ADC is also depicted in Fig. 6.7.2. The active period of the S-CMP is shortened drastically by power gating. The active duty is only 10% of 1H and this can reduce the average current from 4.5 to 1.6μA. Although the LA circuit is fully activated, the power overhead is only 15% of the total power, which is much smaller than saved power.

Figure 6.7.3 shows the circuit schematic of the MS-PGA. A CBSC in [5] consists of two stacked MOS capacitors (MOSCAPs) C_{conv1} and C_{conv2}, a current source and a static comparator. The PGA gain is expressed as $(C_{conv1}+C_{conv2}+C_{para})/(C_{conv2})$, where C_{para} is a parasitic capacitance of a MOSCAP, and the variation of C_{para} seriously degrades column fixed-pattern noise (FPN) characteristics. Another drawback is an overshoot voltage caused by the decision delay of the comparator. The overshoot voltage is accumulated with the number of integration steps, resulting in a large offset. This requires the extra input range of the SS-ADC. The PGA operates as follows: At the beginning of each integration, two current sources charge to C_{CP1} and C_{CP2} until the output of the comparator turns. Although C_{CP1} is reset with RST1 every integration, C_{CP2} is reset with RST2 only once. Charges are accumulated at C_{CP2} depending on the number of integration steps. The MS-PGA has three key features. (1) To cancel out the effect of parasitic capacitance, the SC integrator is implemented with two identical CPs and a comparator. The gain is calculated as $M*(I_{CP2}/I_{CP1})*(C_{CP1}+C_{para})/(C_{CP2}+C_{para})=M$, where $C_{CP1}=C_{CP2}=500fF$ and $I_{CP1}=I_{CP2}=500nA$. (2) Error averaging sufficiently reduces column-to-column gain variation, which is induced by mismatch between I_{CP1} and I_{CP2}. This averaging is realized by switching I_{CP1} and I_{CP2} with every integration and achieves small gain error of σ=0.28% at M=2. (3) The overshoot reduction is performed by accumulating the overshoot voltage to C_{CP2} and flipping C_{CP2} before signal integration. This technique reduces the overshoot voltage from 608 to 336mV for M=16.

Fig. 6.7.4 shows the schematic diagram of the SS-ADC. The LA circuit predicts the level of the pixel signal in advance using the PGA output and additional ramp wave (V_{LA}). The LA circuit is realized with a dynamic comparator (D-CMP) operating at a low frequency of 7.3MHz. The S-CMP is active only from the decision time of the D-CMP to until the S-CMP finishes its decision. The kickback noise occurs when the S-CMP is turned on and off, and is injected to the V_{RAMP}, resulting in a decision error of S-CMP. To suppress the noise, (1) negligible current flows when S-CMP is turned off to reduce the voltage fluctuation V_{RAMP}, and (2) a clock with different phase is input to each column D-CMP to distribute the noise [1]. This gating technique is also applied to the counter, and the high-speed clock operating the counter is gated until the decision of the D-CMP. This can cut the power consumption of the column SS-ADC by reducing the power of the S-CMP by 58% at dark-light illumination without degrading temporal noise.

Figure 6.7.7 shows the chip micrograph of the fabricated CIS, and the cross-section. Each chip size is 5.07mm(H)×3.20mm(V). The top chip and the bottom chip are fabricated with a 65nm CIS and a 65nm CMOS process, respectively. The supply voltages are 2.5V (analog), 1.8V (IO) and 1.2V (digital). The pixel size is 1.12μm(H)×1.12μm(V). In this work, one out of every 8 column pixels is selected with an analog MUX and be connected to column readouts. Figure 6.7.6 shows the 8Mpixel sample photo of this work at M=16, synthesized from eight 1Mpixel frames.

The measured temporal noise with respect to the value of M is shown in Fig. 6.7.5. The temporal noise reduction is almost proportional to the square root of M. The developed CIS achieves a low temporal noise of 1.2e⁻ with M=32 at 20fps. The performance summary at M=16 is shown in Fig. 6.7.6, along with recent CIS with multiple-sampling schemes. The developed CIS consumes 81mW at 24fps and 1Mpixel.

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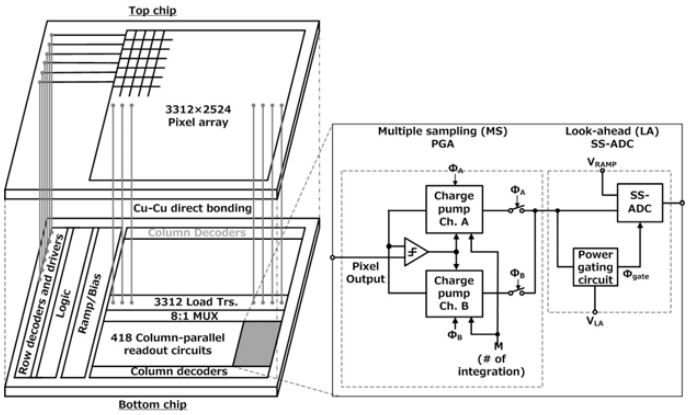


Figure 6.7.1: Structure of 3D-stacked CMOS image sensor.

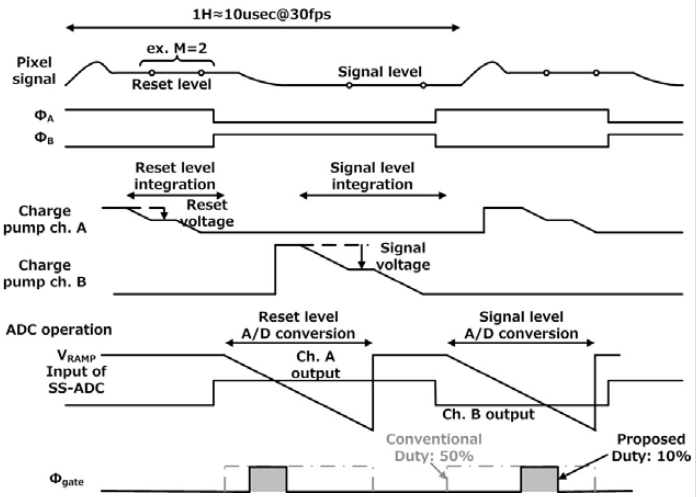


Figure 6.7.2: Timing diagram of the column readout circuit (with overshoot reduction off).

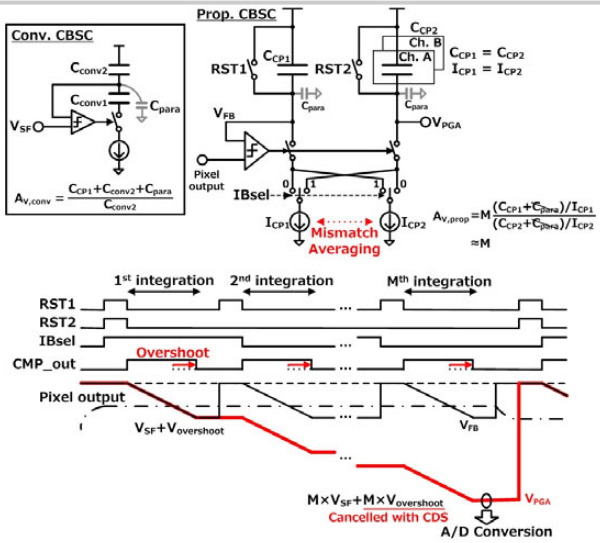


Figure 6.7.3: Circuit schematic and timing diagram of multiple-sampling based CBSC PGA (with overshoot reduction off).

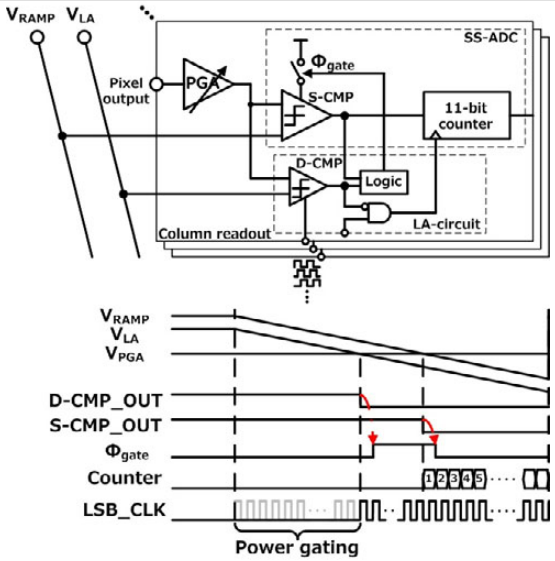


Figure 6.7.4: Circuit schematic and timing diagram of look-ahead SS-ADC.

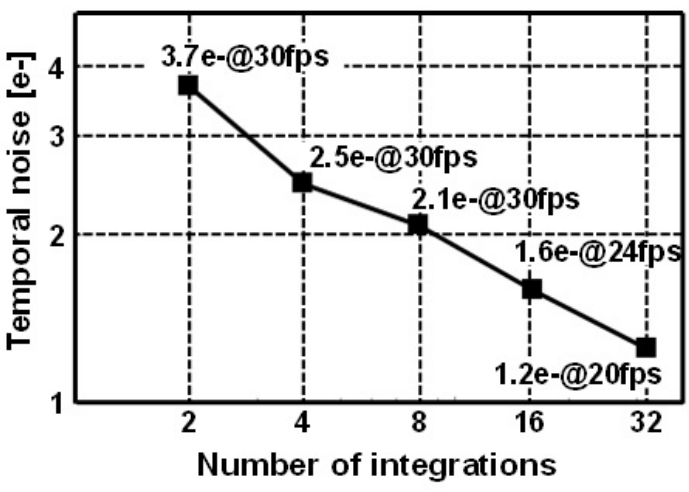


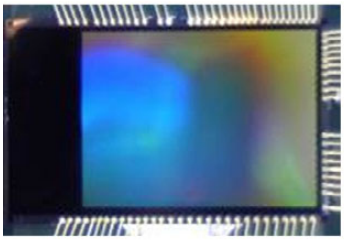
Figure 6.7.5: Measured noise reduction characteristic of proposed CMOS image sensor.

Reference	ISSCC'15 [4]	ISSCC'12 [2]	JSSC'12 [3]	ISSCC'10 [1]	This work	
ADC architecture	SS	FI-Cyclic	FI-Cyclic	ΔΣ	PGA + SS	
Process	90nm/65nm	0.13um	0.18um	0.13um	65nm/65nm	
Supply voltage	2.9V/1.8V/1.1V	4.5V/1.8V/1.5V	3.3V/1.8V	2.8V/1.2V	2.5V/1.8V/1.2V	
# of pixels [pixels]	20M	24M	1M	2.1M	1M*	
Pixel pitch	1.43um	3.9um	7.5um	2.25um	1.12um	
# of sampling	2	32	64 128	130	16	32
Total power [mW]	532	1650	450	180	81	104
Frame rate [fps]	30	10.2	4 2.2	120	24	20
Random noise [e-]	1.3	N/A	1.2 0.95	1.9	1.6	1.2
Power eff. [W/pix/s]	0.86n	6.70n	106n 194n	0.73n	3.23n	4.98n
FoM [W*e-/pix/s]	1.11n	N/A	128n 184n	1.39n	5.17n	5.97n

* 1MPixel out of full 8MPixel are selected with analog MUX

8Mpixel Image

Figure 6.7.6: Performance summary with comparison and sample picture with M=16 mode.



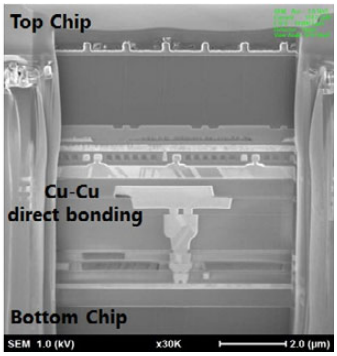


Figure 6.7.7: Chip micrograph and cross-section of 3D-stacked CMOS image sensor.

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6.8 A 1.5V 33Mpixel 3D-Stacked CMOS Image Sensor with Negative Substrate Bias

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3D stacking and computational imaging are two major driving forces for CMOS image sensors. In addition, 3D stacking separates pixel array and peripheral circuits. As such, computational imaging blocks (stereo vision, array camera, reconfigurable instruction cell array, etc.) can integrate with sensor circuits while leveraging advanced CMOS technologies including FinFET. To accommodate this trend, we need to design blocks such as comparators, readouts, transmitters, and PLLs, using digital architectures in logic processes with a minimum number of resistors and capacitors.

Achieving 100% array-to-chip area ratio is an ultimate goal of 3D CIS. For this reason, all peripheral circuits must be under the pixel array. However, row and column circuits may overlap at the corner if both pitches are equal to pixel pitch. To avoid this issue, we make row and pixel pitch the same, and shrink column pitch to 82% to spread the column signal to array width using the "river routing" tools introduced for display-driver ICs, as shown in Fig. 6.8.1. The 3D stacking technology we apply [1] is top-metal face-to-face, and it can put 3D connections under a backside-illuminated pixel array. Therefore it increases array-to-chip area ratio comparing with a TSV chip that uses area outside the pixel array. This chip demonstrates the 3D connections at the center of the uniform 33Mpixel array and seamless image readout using 4 identical 8.3Mpixel circuit units. Instead of developing new circuitry, we can combine 16 compact units for 133Mpixel at the same frame rate and save the extra driving power.

Figure 6.8.2 shows the architecture of the digitally oriented readout circuit. One of the benefits of the 3D chip-stack is that the pixel substrate can be isolated from circuit ground, so we apply a negative bias of -1.3V to the pixel substrate, and decrease the SF supply voltage (V_{pix}) from 2.8 to 1.5V to reduce power consumption from all SF current branches by 46% and to allow operation at the low supply voltages of advanced CMOS technologies. We can also adjust the negative pixel substrate to extend the V_{pin} range and full-well capacity (FWC). On the circuit wafer, the SF current bias is realized by a Native NMOS, which facilitates sufficient headroom for signal swing at 1.5V V_{pix} and better RTS performance by light surface doping. We use a single-slope column ADC, and digital core device single-ended inverter as a high-speed and low-power comparator. The comparator consumes no static current and only 3μW power with minimum RTS in short transient, has customized layout in small column pitch, and always flips at auto-zero level without signal-dependent offset. The cascode MOS isolates the kick-back noise and activates different current branches to adjust comparator g_m and bandwidth. The customized 3-terminal interlaced MOM capacitor is a charge-summing structure that serves as a level shifter to protect the core device.

For each column, a Gray-Binary hybrid counter [2] counts from the voltage ramp start until the comparator flips its state, which corresponds to the SF output level. The intrinsic 5b Gray-code counter utilizes both rising and falling clock edges to count at a maximum 2.12GHz. Every column has a 5b latch to track the Gray-code counter. The MSB of the latch drives the subsequent 8b binary ripple counter. Whenever the comparator flips to hold the latch value, the binary counter also stops and both wait for data shift. There are 11 Gray-code counters and each one is shared by 150 column latches for 2×2 half-line readout. The PLL clock is delivered to 11 Gray-code counters spread across the entire column circuit width, and the delay is cancelled by digital CDS. To minimize the duty cycle degeneration of the clock transfer, there is a clock phase inversion option between every 2 Gray-code counters for calibration.

The voltage ramp is generated by I*R or I/C mode. The I/C is preferred for low power and without external components. The ramp slope is positive and saves one reference voltage by using ground. The current switches are digitally controlled to output various values at different time periods, so it realizes a voltage ramp with multiple adjustable piecewise linear slopes (multi-slope) that can be used to calibrate the system linearity. Figure 6.8.3 shows the measurement results. The DNL is <0.3 LSB. Raw data INL is up to 40 LSB due to the nonlinearity of the parasitic capacitor. By using multi-slope, the INL can be calibrated to <4 LSB by 6 segments of slope adjustment. The RN histograms show the counter, comparator, and SF input random noises. The hybrid counters show almost-zero RN except some columns at Gray code boundary depending on its location and clock delivery. The comparator input RN is 82.35μV_{rms} at 1× gain. For SF input RN histogram, the TX is turned off and the floating diffusion node is connected to V_{pix} at 1.5V through the RST device. The result shows the Native NMOS bias has better RTS performance.

Figure 6.8.4 shows two raw images captured by voltage ramp of single-slope (top) and multi-slope (bottom) approaches. With single-slope, the right LEGO room is too dark to see the objects when the slope is large at 1× gain. If we apply high gain with smaller slope, the dark room emerges but the left bright room (with LED on the roof) is saturated. Both high-gain and low-gain regimes lose image information and the later digital gain (gamma correction) does not help. With multi-slope, it is regarded as an analog gamma correction. The dark side information is resolved as well as with high analog gain, and the bright side is not saturated since multi-slope maintains the same signal range. The bright region is dominated by shot noise so the resolution can be relaxed. It preserves most information and uses the minimum power compared with digital HDR synthesis, especially suitable for low-power computational imaging and IoE applications.

To minimize the pin count of each readout unit, we apply a clock embedded transmitter (8b10b encode as same as MIPI CSI-3) and use an HDMI cable (4 lanes for 4 CIS units) with a 2.5Gb/s/lane FPGA receiver. In Fig. 6.8.5, the serializer has a a 10-DFF shift register to form the 1/20 divider in a PLL loop to generate a 125MHz system PCLK. Another 2 groups of the 10-DFF shift registers work by the Ping-Pong principle: while one loads the parallel data by 125MHz PCLK_90, the other shifts data out by 2.5GHz DCO_CLK. The all-digital PLL uses a digital PID controller to replace the RC loop filter and output the control code to a digitally controlled oscillator. The input of the PID controller is the UP/DN codes that are digitized from a classical phase & frequency detector (PFD) output. It is digitized by rising edge to start propagation, and by falling edge to latch the propagated value responding to the UP/DN pulse width. By the F_{ref}-controlled latch scheme, the PID controller outputs the corresponding code with one reference clock cycle latency. This architecture requires no FIFO line buffer between the sensor and serializer, since all circuits are in the same clock domain.

Figure 6.8.6 shows the specifications and comparison table. For 8Mpixel [3,4], it shows that the digitally oriented, inverter-type single-ended comparator has lower random noise and power. The 2D prototype and 3D unit both use the same circuits except the transmitter and MOM capacitor. The power is further reduced by using 1.5V V_{pix} and the clock embedded transmitter. The 3D connections underneath the pixel array drastically improve the array-to-chip area ratio to 82.5% (if 100% required, the I/O bond PAD need to put on the other side of wafer). The frame rate is designed for the Camera-Link frame grabber system (33Mpixel × 12b × 15fps ~= 6Gb/s), but it operates at half speed due to FPGA RX development and PCB signal integrity status. The 1/4 data bandwidth is not used since TX transmits every 16b data, including 4b reserved for future extension. To compare with larger array sensors [5,6], this work shows a linear increase in (low) power and small area with high flexibility. Figure 6.8.7 shows the chip diagram, the pin count of each 8.3Mpixel unit is only 17, and the 33Mpixel imager uses a 68pin CLCC package.

Acknowledgement:
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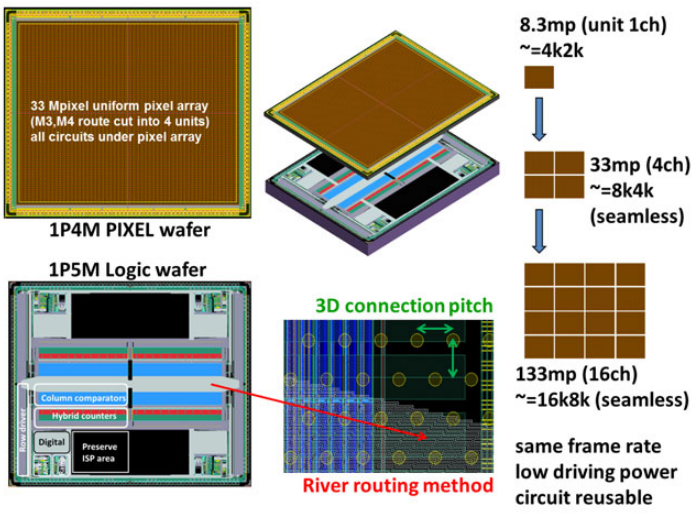

Figure 6.8.1: 3D stacked and 33Mpixel array readout by 4 identical units.

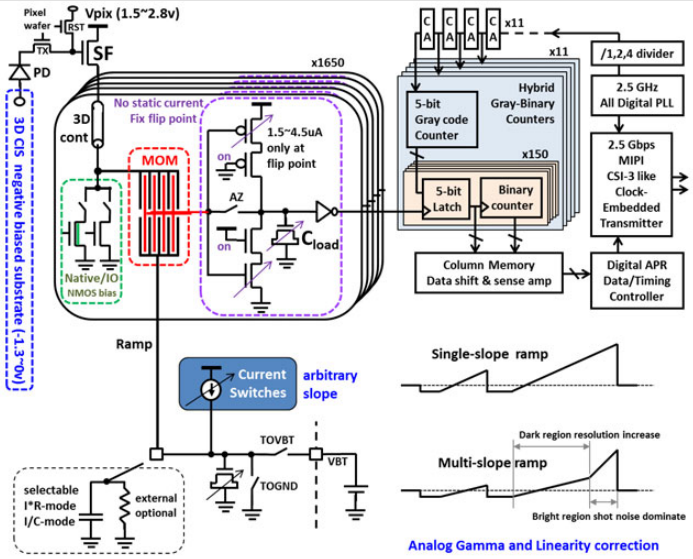

Figure 6.8.2: Digitally oriented sensor readout architecture.

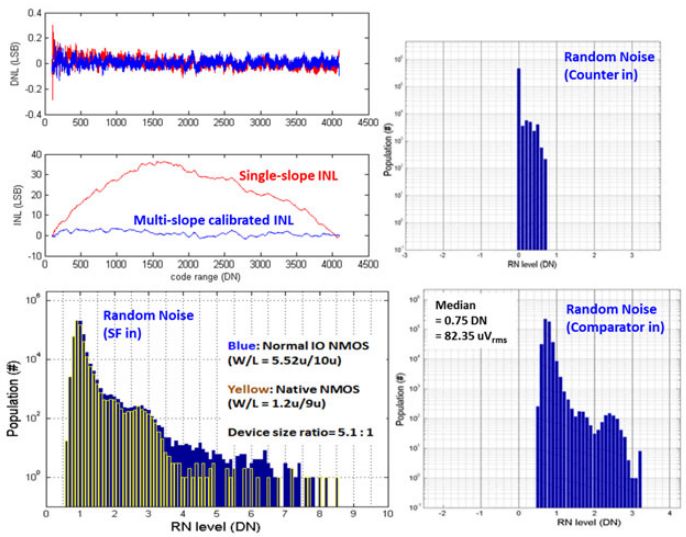

Figure 6.8.3: Linearity and random noise histogram of counter, comparator, and SF input.

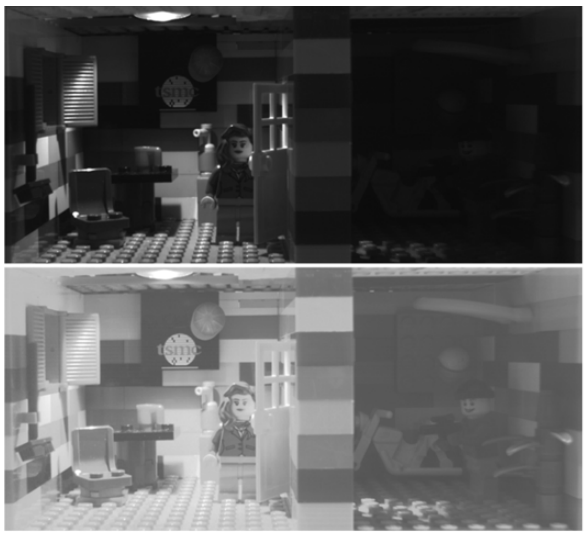

Figure 6.8.4: Raw image by single-slope (top) & multi-slope (bottom) of voltage ramp.

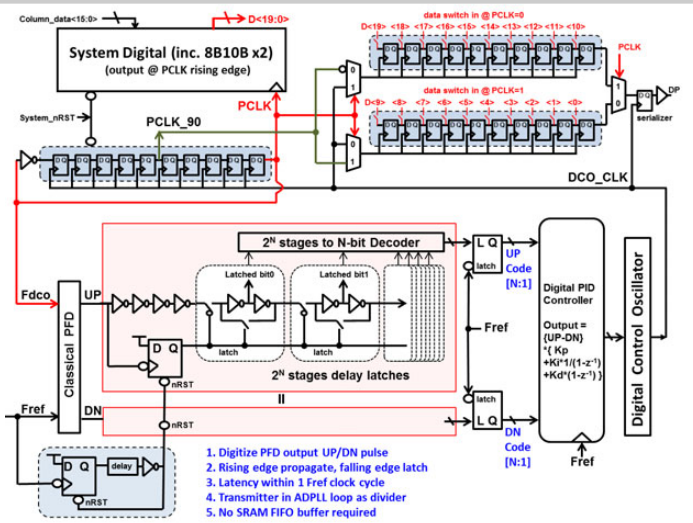

Figure 6.8.5: Clock embedded data serializer and all-digital PLL with digitized UP/DN pulse.

	8Mpixel comparison		This Work			Larger Mpixel comparison	
	[3]	[4]	Prototype (2D)	unit (3D)	whole chip (3D)	[5]	[6]
Pixel count	8 mp	8.08 mp	8.28 mp	8.28 mp	33 mp	20 mp	133 mp
Technology	90nm 1p4m 2D	65nm 1P7M 3D TSV	65nm 1P5M 2D	65nm 1P5M 3D connection under array		65nm 1P7M 3D TSV	0.18um 1P4M 2D
Image size	1/3.2 inch	1/4 inch	1/4 inch	1/4 inch	1/2 inch	1/1.7 inch	1.7 inch
resolution (full frame)	N/A	3280 x 2464	3296 x 2512	3296 x 2512	6592 x 5024	5256 x 3934	15488 x 8776
Supply Voltage	N/A	2.7 V / 1.05 V	2.8 V / 1.2 V	1.5 V (up to 2.8 V) / 1.2 V		2.9 V/1.8 V/1.1 V	3.3 V / 1.8 V
ADC architecture	Pseudo Multiple Sampling	Single Slope	Single Slope, Single-Ended			Single Slope, Multiple Sampling	32-shared SAR ADC x 484
ADC resolution	10 bit	10 bit	12 bit			12 bit	12 bit
Readout ckt. Random Noise	134 uVrms (M=16)	139 uVrms (18dB Again)	83.4 uVrms (1x Again)	82.35 uVrms (1x Again)		99.6 uVrms (27dB, M=2)	281.6 uVrms (3x PGA gain)
Frame rate (full frame)	15 fps	30 fps	15 / 7.5 fps*	15 / 7.5 fps*		30 fps	60 fps
Data rate (full frame)	130 MHz parallel	750 Mbps serial 4 lane + clk lane	896/448 Mbps* serial 2 lane + clk lane	2.5/1.25 Gbps* serial 1 lane clk-embedded	2.5/1.25 Gbps* serial 4 lane clk-embedded	2.3 Gbps serial 8 lane clk-embedded	1.15 Gbps 112 lane + clk lane
Power (full frame)	280 mW	185 mW	52mW	45 mW	180 mW	532 mW	11000 mW
Array-to-Chip area ratio (%)	44.8 %	64.2 %	30 %	82.5 %		67.8 %	43.9 %

* Note: Subject to FPGA receiver development & PCB signal integrity status, all measured data operate at half speed for better stability.

Figure 6.8.6: Specification and performance comparison.

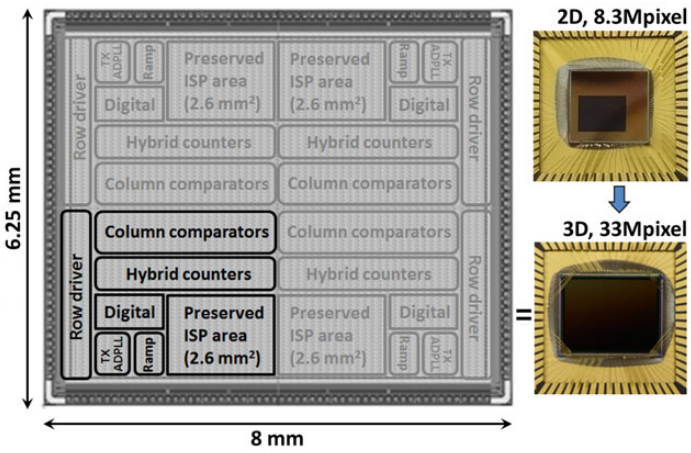

Figure 6.8.7: Chip photograph with 68-pin CLCC package.

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6.9 A 1.1μm 33Mpixel 240fps 3D-Stacked CMOS Image Sensor with 3-Stage Cyclic-Based Analog-to-Digital Converters

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There is an increasing demand for high-reality video systems. The ITU-R has standardized video parameters for ultra-high-definition TV (UHDTV), and the full-specification video signal stated in this international standard is prescribed as having a 7,680 (H) × 4,320 (V) pixel count, 120Hz frame frequency with progressive scanning, 12b tone reproduction, and wide color gamut. A 33Mpixel 120fps CMOS image sensor with a 12b column-parallel analog-to-digital converter (ADC) is reported in [1]. In addition to standard operation, higher sensitivity, smaller pixels, and a higher frame rate of 240fps or more are required for CMOS image sensors. Backside-illuminated stacked CMOS image sensors [2] are effective for simultaneously achieving both high sensitivity for small pixels and high operation speed. However, these stacked structures are still insufficient for high-frame-rate UHDTV image sensors since the pixel wafer and the ASIC wafer are connected by through-silicon vias in the peripheral area.

This paper describes a 1.1μm-pitch 33Mpixel 240fps 3D-stacked CMOS image sensor with a 3-stage cyclic-based ADC. We report a narrow-pitch hybrid-stacking technology between the pixel wafer and the ASIC wafer that connects inside the pixel area. The 3D-stacked architecture, built by hybrid-stacking technology, makes it possible to place a 1,932 (H) × 4 (V) CDS/ADC array underneath the pixel area and also reduces the pixel random noise because the pixel wafer is independently tuned from the ASIC wafer. Furthermore, the pipelined and parallel operation of the 3-stage cyclic-based ADC effectively reduces the conversion time and power consumption and achieves 12b precision within 1 horizontal scan time of 0.92μs at 240fps. As a result, a low noise of 3.6e^- and a low power consumption of 3.0W are attained at a high pixel rate of 7.96Gpixel/s, and a good figure of merit (FOM) is achieved compared with recently published image sensors.

Figure 6.9.1 shows a 3-dimensional illustration of the backside-illuminated 3D-stacked CMOS image sensor. The process of fabricating the pixel wafer is optimized for low random noise. Conversely, that of the ASIC wafer is optimized for high-speed operation of readout circuits by forming shallow junctions. The pixel wafer is stacked face-to-face on the ASIC wafer by a hybrid-stacking process, followed by the thinning-down process to the target thickness. The sensor has 50Mpixel/190fps and 33Mpixel/240fps modes. The pixel wafer of the chip has a total of 9,600 (H) × 5,396 (V) with 1.1μm-pitch 2×2-shared pixels. The effective pixel array is 7,728 (H) × 4,368 (V) for 33Mpixel/240fps mode. The ASIC wafer of the chip has a 1,932 (H) × 4 (V) CDS/ADC array composed of a current source load (CSL), a correlated double sampling (CDS) with an analog gain amplifier of up to 4.0, and a 12b 3-stage cyclic based ADC, all of which are located underneath the pixel array. A 4×4-pixel unit has 4 sets of 2×2-shared pixels and repeats along the column direction in 4 (H) × 4,368 (V) pixels. Each 4 sets of 2×2-shared pixels share output lines and connect with 4 CDS/ADCs, which are placed along the column direction. The horizontal pitch of the CDS/ADC and the hybrid-stacking interconnection is selected to be 4.4μm in consideration of manufacturability, sensor specifications, ADC architecture, and pixel size. There are a total of 20 blocks of horizontal scanners, current-mode logic (CML) circuits, digital processing circuits, and scalable low-voltage signaling (SLVS) drivers, and each of the 10 blocks are located on the top and bottom of the CDS/ADC array. The 12 middle blocks have an active 480 columns, and 4 right and 4 left side blocks have an active 270 columns. The binary data output from 3 ADCs are combined into the 12b binary data, and the parallel 12b data is converted to serial data in the digital processing circuits. Each block has 6-fold parallel 1.2Gb/s SLVS output ports; therefore, in total 120 ports output an aggregate data rate of 144Gb/s.

Figure 6.9.2 shows the architecture of the 12b 3-stage cyclic-based ADC. This ADC is composed of a first single-ended cyclic ADC that converts the upper 3b, a second single-ended cyclic ADC that converts the middle 6b, and a third successive-approximation resistor (SAR) ADC that converts the lower 3b. In previous work [1], a two-stage pipelined operation of the first 4b and second 8b cyclic ADCs was applied to a 33Mpixel 120fps CMOS image sensor, and its high efficiency for high-speed low-power operation was demonstrated. The three-stage ADC of this paper relaxes the clock speed of the cyclic ADCs required for 240fps operation while maintaining low power by using the SAR ADC as the third stage. Conventional N-bit SAR ADCs need a 2^N layout area of capacitors for the successive-approximation operation; therefore, a SAR ADC with a large number of bits is difficult to design in a small layout area. We successfully reduce the layout area of capacitors to $2^{(N-1)}$ by adding a reference voltage (V_{RC}), where $V_{RL}<V_{RC}<V_{RH}$. We carefully design the bit allocation for each ADC considering the balance of the operation speed, power consumption, and layout area. The first and second cyclic ADCs output a 1.5b redundant binary code because it can reduce the demand for precision of the comparator. Then, all binary codes from 3 ADCs are joined up to generate a 12b code in the digital processing circuits. We used a SPICE simulation to estimate the power consumption of the designed 3-stage cyclic-based ADC, and it was 120μW while realizing a conversion time period of 0.92μs. This conversion time period is half, and the power consumption is almost the same compared with the previously designed 2-stage cyclic ADC [1]. Thanks to this SAR ADC design and the fine process technology, the layout area of the 3-stage cyclic-based ADC is 4.4μm (H) × 920μm (V), which enables the placing of 4 CDS/ADCs along the column direction.

Figure 6.9.3 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the implemented 12b 3-stage cyclic-based ADC. DNL is +0.82/-0.88 LSB at a 12b resolution at 240fps, which means that there is no missing code. INL is +1.04/-11.75 LSB, which means that the variation is to within 0.31% of the video signal range.

Figure 6.9.4 lists the performance of the image sensor. The pixel wafer of the chip is fabricated using a 45 nm 1P4M MOS process, and the ASIC wafer of the chip is fabricated using a 65 nm 1P5M logic process. The image size is 8.448mm (H) × 4.752mm (V). The supply voltages are 1.2/2.5V for digital and 2.5/2.8V for analog. The maximum frame rate is 240fps. The conversion gain of the pixel is 92μV/e^-, sensitivity is 0.55V/lx-s without a color filter and micro lens, and full-well capacity is 5,700e^-. Random noise of 3.6e^- rms is obtained at an analog gain of 4.0 and a pixel rate of 7.96Gpixel/s. The pixel rate is defined as (number of pixels × fps). The total power consumption is 3.0W.

Figure 6.9.5 shows a captured image. In the image, no dead-line error is detected. This means that all hybrid stackings are interconnected. The magnified center image is also shown in Fig. 6.9.5, indicating a resolution of more than 3,200 TV lines.

Figure 6.9.6 lists a comparison of the performance of recently published image sensors [1,3–6]. An FOM1 of 1.36e^-nJ and an FOM2 of 1.32e^-pJ/step are achieved when FOM1 and FOM2 are defined as (power × noise × 10^9)/(number of pixels × fps) and (power × noise × gain × 10^{12})/(number of pixels × fps × 2^{bits}), respectively. These FOMs of the fabricated image sensor are comparable or better than those of others, while attaining an extremely high pixel rate of 7.96Gpixel/s. A micrograph of the chip is shown in Fig. 6.9.7.

Acknowledgements:
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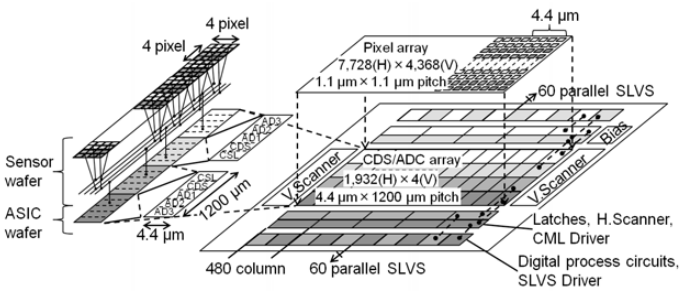

Figure 6.9.1: Structure of stacked CMOS image sensor.

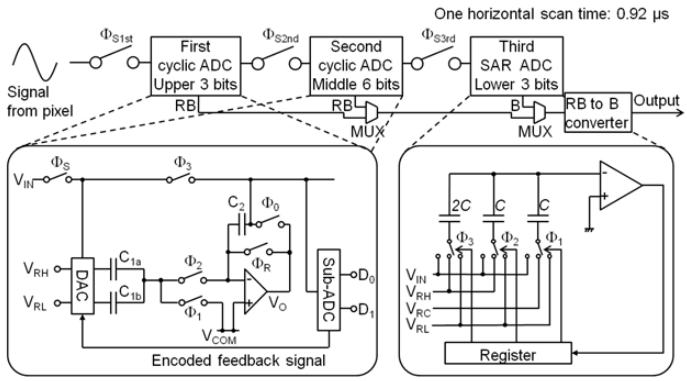

Figure 6.9.2: Diagram of 12b cyclic-cyclic-SAR ADC.

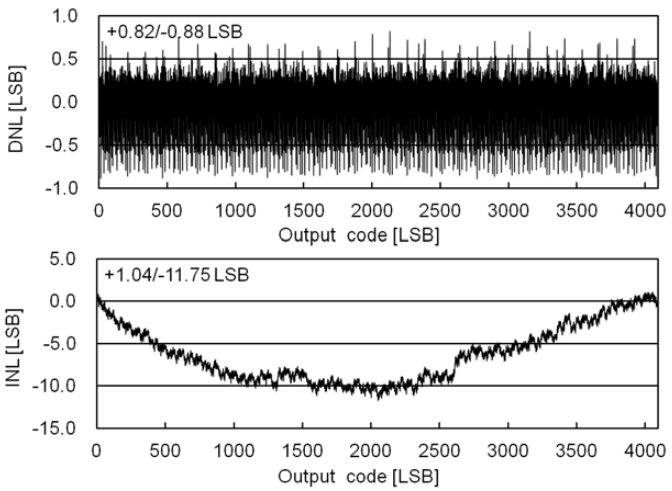

Figure 6.9.3: Measured DNL and INL at 240fps.

Fabrication process	45 nm 1P4M pixel / 65 nm 1P5M logic
Image size	Diagonal 9.693 mm
Supply voltage	1.2/2.5 V (digital), 2.5/2.8 V (analog)
Number of total pixels	9,600 (H) × 5,396 (V)
Number of effective pixels	7,728 (H) × 4,368 (V)
Pixel size	1.1 μm × 1.1 μm
Pixel type	1.75-Tr. 2 × 2-shared pixel
Frame rate	240 fps (maximum)
ADC resolution	12 bit
ADC DNL	+0.82/-0.88 LSB
ADC INL	+1.04/-11.75 LSB
Conversion gain	92 μV/e-
Sensitivity	0.55 V/lx-s (w/o ML & CF, CIE A-light)
Full well capacity	5,700 e-
Random noise	4.5 e-rms (gain: 1.0) at 240 fps 3.6 e-rms (gain: 4.0) at 240 fps
PRNU	< 1.3% (Dead-line free)
Power consumption	3.0 W at 240 fps

Figure 6.9.4: Specifications summary.

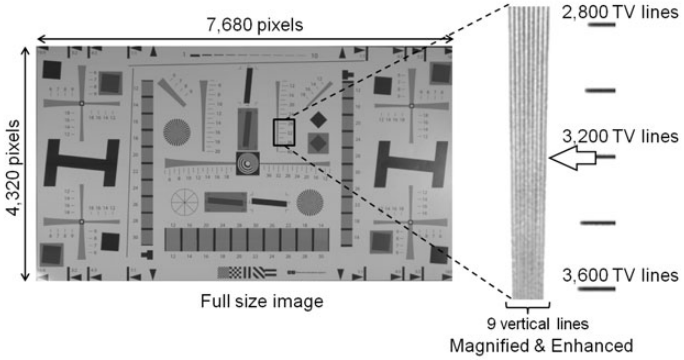

Figure 6.9.5: Reproduced full-size image.

	Ref.[3]	Ref.[1]	Ref.[4]	Ref.[5]	Ref.[6]	This work
ADC type	SS	2-stage cyclic	SAR	SS	SAR	3-stage cyclic based
ADC resolution [bit]	12	12	12	12	12	12
Frame rate [fps]	120	120	80	30	60	240
# of H. pixels	8192	7680	4620	5256	15360	7680
# of V. pixels	2160	4320	3084	3934	8640	4320
Random noise [e-rms]	2.75	3.0	1.7	1.3	7.68	3.6
Gain	11.2	7.5	17.8	22.4	2	4.0
Power consumption [W]	3	2.67	1.1	0.532	11	3.0
FoM1 [e-・nJ]	3.89	2.01	1.64	1.11	10.61	1.36
FoM2 [e-・pJ/step]	10.62	3.68	7.13	6.10	5.18	1.32

Figure 6.9.6: Performance comparison.

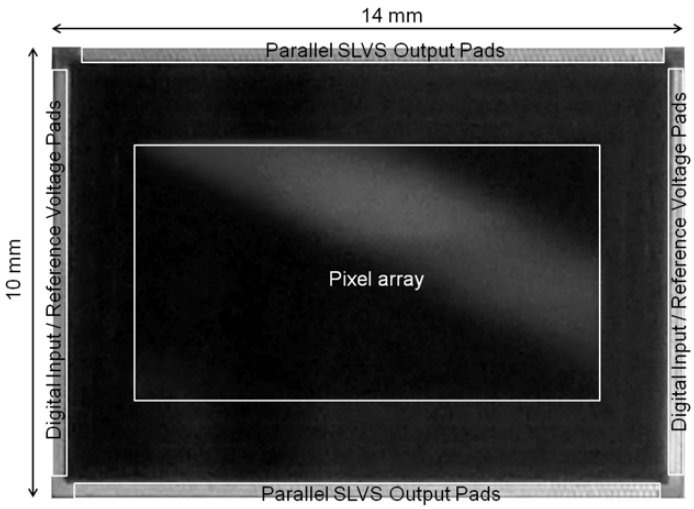

Figure 6.9.7: Chip microphotograph.

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